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STEP TECHNICA CO.,LTD.

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CUnet

CUnet IC MKY43

User's Manual

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Preface

This manual describes the MKY43, or a kind of CUnet IC.
Be sure to read ***"CUnet Introduction Guide"*** before understanding this manual and the MKY43.

● **Target Readers**

This manual is for:

- Those who first build a CUnet
- Those who first use StepTechnica's various ICs to build a CUnet

● **Prerequisites**

This manual assumes that you are familiar with:

- Network technology
- Semiconductor products (especially microcontrollers and memory)

● **Related Manuals**

- CUnet Introduction Guide
- CUnet Technical Guide

[Caution]

- Some terms in this manual are different from those used on our website and in our product brochures. The brochure uses ordinary terms to help many people in various industries understand our products.
  Please understand technical information on HLS Family and CUnet Family based on technical documents (manuals).

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CONTENTS

Chapter 1 MKY43 Role and Features

1.1 CUnet Station in MKY43 (MEM Station) 1-3
1.2 Features of MKY43 1-4
1.3 Connection to I/O Station 1-5

Chapter 2 MKY43 Hardware 2-3

Chapter 3 Connecting MKY43

3.1 Voltage Levels of Pins Connecting to Signal Pins 3-4
3.2 Supplying Driving Clock and Hardware Reset Signal 3-6
3.2.1 Supply of Driving Clock 3-6
3.2.2 Supply of Hardware Reset Signal 3-6
3.3 Connecting Network Interface 3-7
3.3.1 Recommended Network Connection 3-7
3.3.2 Details of RXD, TXE, and TXD Pins 3-7
3.4 Setting Baud Rate 3-8
3.5 Network Cable Length 3-9
3.6 Setting Station Addresses and Owned Area 3-10
3.7 Connecting LED Indication Pins 3-10
3.8 Connection of UTY1 Pin and UTY2 Pin 3-11
3.8.1 Details of #CYCT Signal 3-12
3.8.2 Details of #PING Signal 3-12
3.9 Connecting User Bus 3-13
3.9.1 Data Storage Method 3-13
3.9.2 Function of #SWAP Pin 3-13
3.9.3 Connection to 16-bit User Bus 3-14
3.9.4 Connection to 8-bit User Bus 3-15
3.9.5 Recognition of Access 3-16
3.9.6 Design of Access Time 3-16
3.9.7 Access Tests after Embedding MKY43 3-17
3.9.8 Interrupt Trigger to CPU 3-17

Chapter 4 MKY43 Software

4.1 Start and Stop of Communication 4-3
4.1.1 Memory Map 4-4
4.1.2 Checking Connection of MKY43 4-4

4.1.3 Initialization and Start-up of Communication 4-5
4.1.4 Responses to Each Phase 4-6
4.1.5 Protection against Misoperation 4-7
4.1.6 Cycle Time of CUnet 4-8
4.1.7 Detailed Timing during Cycle 4-8
4.1.8 Network Stop 4-9
4.1.8.1 Details of SNF (Station Not Found) 4-9
4.1.8.2 Details of OC (Out of Cycle) 4-10
4.1.8.3 Stop Exception 4-10
4.2 Use of GM 4-11
4.2.1 Details of Owned Area 4-11
4.2.2 Data Hazards 4-12
4.2.2.1 Hazard Protection Function 4-14
4.2.2.2 How to Use Read Hazard Protection 4-14
4.2.2.3 How to Use Write Hazard Protection 4-15
4.2.2.4 Protection Against Data Hazard without Hazard Protection Function 4-16
4.2.3 Quality Assurance of GM Data 4-17
4.2.3.1 Status Indication by Registers 4-17
4.2.3.2 Starting Point of Status Management and Exception 4-18
4.2.3.3 Link Group Register (LGR) 4-19
4.2.3.4 Member 4-20
4.2.3.5 Member Flag Register (MFR) 4-21
4.2.3.6 Member Group Register (MGR) 4-21
4.2.3.7 Detection of Member Increase and Decrease 4-23
4.2.4 Detection of Global Memory Data Transition 4-24
4.2.4.1 Data Renewal Check Register (DRCR) for Setting Detection of Data Transition 4-24
4.2.4.2 Transition Timing of DR Flag Bit and DRFR Bits from "0" to "1" 4-25
4.2.4.3 Transition Timing of DR Flag Bit and DRFR Bits from "1" to "0" 4-25
4.2.4.4 Precautions for Use of Detection of Data Transition 4-27
4.3 Use of Mail Sending/Reception Function 4-28
4.3.1 Permission for Mail Reception 4-29
4.3.2 Operation for Mail Reception 4-30
4.3.3 Operation for Mail Sending and after Completion of Sending 4-32
4.3.4 Operation against Mail Sending Errors 4-34
4.3.5 Quality Assurance for Mail Sending/Reception 4-35
4.3.6 User-support Functions in Mail Sending/Reception 4-35
4.3.7 Estimation of Mail Sending/Reception Time 4-35
4.3.8 Precautions for Mail Sending/Reception 4-36
4.4 Detailed Operation and Management of CUnet System 4-37
4.4.1 Monitoring before Network Start 4-38
4.4.2 Resizing of Cycle Time 4-39
4.4.2.1 Resizing 4-40
4.4.2.2 Rejection of Resizing 4-41
4.4.2.3 Resize Overlap (RO) 4-42
4.4.2.4 Caution when RO Occurs 4-42

4.4.3 Detection and Handling of CUnet Station in BREAK Phase 4-43
4.4.4 Detection and Handling of Jammer 4-44
4.4.5 Controling and Monitoring Network Quality 4-45
4.4.5.1 LCARE Signal Output 4-45
4.4.5.2 MCARE Signal Output 4-46
4.4.5.3 MON Signal Output 4-47
4.4.6 PING Instruction 4-48
4.4.7 Function to Detect Mode of Each Station 4-49
4.4.8 Global Memory Monitor (GMM) Function 4-50
4.4.9 Frame Option [for HUB] 4-51
4.4.9.1 Number of Insertable HUBs 4-52
4.4.9.2 Setting of Frame Option 4-53
4.5 Interrupt Trigger Generation Function 4-54
4.5.1 Operation of #INT0 Pin 4-54
4.5.2 Retrigger Function 4-56
4.5.3 Interrupt Factors 4-57
4.5.4 Operation of #INT1 Pin 4-58
4.5.5 Precautions for Specifying Timing of Interrupt Trigger Generation 4-58
4.5.6 Precautions for Use of Data Renewal (DR) Interrupt Trigger 4-58
4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation 4-59
4.5.8 BD/RO/JD Interrupt Generation 4-59

Chapter 5 Register Reference

5.1 Receive Flag Register (RFR) 5-5
5.2 Link Flag Register (LFR) 5-6
5.3 Member Flag Register (MFR) 5-7
5.4 Data Renewal Flag Register (DRFR) 5-8
5.5 Link Group Register (LGR) 5-9
5.6 Member Group Register (MGR) 5-10
5.7 Data Renewal Check Register (DRCR) 5-11
5.8 Read Hazard Control Register 0 (RHCR0) 5-12
5.9 Read Hazard Control Register 1 (RHCR1) 5-12
5.10 Write Hazard Control Register 0 (WHCR0) 5-13
5.11 Write Hazard Control Register 1 (WHCR1) 5-13
5.12 Mail Send Limit time Register (MSLR) 5-14
5.13 Mail Send Result Register (MSRR) 5-14
5.14 Mail Error Status Register (MESR) 5-15
5.15 Mail Send Control Register (MSCR) 5-16
5.16 Mail Receive 0 Control Register (MR0CR) 5-17
5.17 Mail Receive 1 Control Register (MR1CR) 5-18

5.18 Care CounTer Register (CCTR) 5-19
5.19 UTility pin Control Register (UTCR) 5-20
5.20 Query Control Register (QCR) 5-21
5.21 New Final Station Register (NFSR) 5-22
5.22 Final Station Register (FSR) 5-22
5.23 Basic Control Register (BCR) 5-23
5.24 INTerrupt 0 Control Register (INT0CR) 5-24
5.25 INTerrupt 1 Control Register (INT1CR) 5-26
5.26 Interrupt Timing 0 Control Register (IT0CR) 5-27
5.27 Interrupt Timing 1 Control Register (IT1CR) 5-27
5.28 INTerrupt 0 Status Register (INT0SR) 5-28
5.29 INTerrupt 1 Status Register (INT1SR) 5-30
5.30 System Status Register (SSR) 5-32
5.31 System Control Register (SCR) 5-34
5.32 Chip Code Register (CCR) 5-36
5.33 Read Hazard Protection Buffer 0 (RHPB0) 5-37
5.34 Read Hazard Protection Buffer 1 (RHPB1) 5-38
5.35 Write Hazard Protection Buffer 0 (WHPB0) 5-39
5.36 Write Hazard Protection Buffer 1 (WHPB1) 5-40

Chapter 6 Ratings

6.1 Electrical Ratings 6-3
6.2 AC Characteristics 6-3
6.2.1 Clock and Reset Timing 6-4
6.2.2 Output Timing of Interrupt Trigger 6-4
6.2.3 Output Timing of #CYCT, #LCARE and #MCARE 6-4
6.2.4 Read/Write Timing 6-5
6.2.5 Baud Rate Timing 6-6
6.2.6 External Baud Rate Clock (EXC) Timing 6-6
6.3 Package Dimensions 6-7
6.4 Recommended Soldering Conditions 6-8
6.5 Recommended Reflow Conditions 6-8

Appendix

Appendix 1 Cycle Time Table App-3
Appendix 2 Differences between MKY43 and MKY40 ..... App-4
Appendix 3 Processing when Network Stop by OC (Out of Cycle) Occurs App-7

Figures

Fig. 1.1 CUnet Station with MKY43 (MEM Station) 1-3
Fig. 1.2 CUnet Connecting Four MEM Stations 1-4
Fig. 1.3 I/O Station 1-5
Fig. 1.4 CUnet Connecting I/O Station 1-5
Fig. 2.1 MKY43 Pin Assignment 2-3
Fig. 2.2 Pin Electrical Characteristics in I/O Circuit Types of MKY43 2-7
Fig. 3.1 Connection Causing Leakage Current 3-4
Fig. 3.2 Hardware Reset 3-6
Fig. 3.3 Recommended Network Connection 3-7
Fig. 3.4 LED Connection 3-10
Fig. 3.5 UTY1 Pin and UTY2 Pin Control 3-11
Fig. 3.6 Differences between Addresses for Byte Access Depending on Endian 3-13
Fig. 3.7 Connection to 16-bit User Bus 3-14
Fig. 3.8 Connection to 8-bit User Bus 3-15
Fig. 4.1 Start Algorithm 4-5
Fig. 4.2 Phase Transition of MKY43 and Corresponding Bits of SCR 4-6
Fig. 4.3 Write Protection 4-7
Fig. 4.4 Station Times Indicated by Bits 0 to 6 of SCR 4-8
Fig. 4.5 Global Memory (GM) 4-11
Fig. 4.6 Expansion of Owned Area 4-12
Fig. 4.7 Mechanism of Data Hazard 4-13
Fig. 4.8 Data Hazards during Writing 4-13
Fig. 4.9 Reading by Using Hazard Protection Function 4-14
Fig. 4.10 Writing by Using Hazard Protection Function 4-15
Fig. 4.11 64-bit RFR and LFR 4-17
Fig. 4.12 Starting Point of Status Management 4-18
Fig. 4.13 LFR Monitoring by LGR 4-19
Fig. 4.14 64-bit MFR and MGR 4-20
Fig. 4.15 MFR Monitoring by MGR and Bit Status of SSR 4-22
Fig. 4.16 64-bit DRCR and DRFR 4-24
Fig. 4.17 Outline of Data Renewal Detection for Time Passage 4-26
Fig. 4.18 Mail Receive Buffers 4-29
Fig. 4.19 Permission for Mail Reception 4-29

Fig. 4.20 MR0CR with Dataset Stored in MRB0 4-30
Fig. 4.21 MR1CR with Dataset Stored in MRB1 4-30
Fig. 4.22 Mail Send Buffer 4-32
Fig. 4.23 Operation of MSLR and MSCR 4-32
Fig. 4.24 MSRR 4-33
Fig. 4.25 MESR 4-34
Fig. 4.26 Resize 4-39
Fig. 4.27 Resizing 4-40
Fig. 4.28 RO Bit of SSR 4-42
Fig. 4.29 BD Bit of SSR 4-43
Fig. 4.30 JD Bit of SSR 4-44
Fig. 4.31 Number of LCARE Occurrences of CCR 4-45
Fig. 4.32 Number of MCARE Occurrences of CCR 4-46
Fig. 4.33 Example of Output to #MON Pin 4-47
Fig. 4.34 Issuing PING Instruction 4-48
Fig. 4.35 Mode Checking for Each MEM Station 4-49
Fig. 4.36 Number of Inserted HUBs 4-52
Fig. 4.37 Setting of Frame Option 4-53
Fig. 4.38 Interrupt Trigger Generating Function 4-54
Fig. 4.39 DR and ALM Interrupt Trigger Generation Timing 4-55
Fig. 4.40 Operation Example of Retrigger Function 4-56
App. Fig. 1 Example of Processing by Polling when Network Stops App-7
App. Fig. 2 Example of Processing by Using Interrupt when Network Stops (1) ... App-8
App. Fig. 3 Example of Processing by Using Interrupt when Network Stops (2) ... App-8

Tables

Table 2-1 Pin Functions of MKY43 2-4
Table 2-2 Electrical Ratings of MKY43 2-6
Table 3-1 Network Cable Length 3-9
Table 4-1 Memory Map 4-4
Table 4-2 Type Codes 4-49
Table 4-3 Interrupt Factors 4-57
Table 4-4 Frozen Registers 4-59
Table 5-1 Register List 5-4
Table 5-2 Bit Definition for UTCR 5-20
Table 5-3 Type Codes at Query Completion 5-21
Table 5-4 Bit Values and Baud Rates (for 48-MHz Clock) 5-23
Table 6-1 Absolute Maximum Ratings 6-3
Table 6-2 Electrical Ratings 6-3
Table 6-3 AC Characteristics Measurement Conditions 6-3

Chapter 1 MKY43 Role and Features

This chapter describes the role and features of the MKY43 in CUnet.

1.1 CUnet Station in MKY43 (MEM Station) 1-3

1.2 Features of MKY43 1-4

1.3 Connection to I/O Station.....1-5

Chapter 1 MKY43 Role and Features

This chapter describes the role and features of the MKY43 in the CUnet.
The MKY43 is a CUnet-dedicated IC with the CUnet protocol (CUnet IC) based on full hard-wire logic packaged in a 64-pin TQFP using CMOS technology. The MKY43 was developed as a product inheriting the MEM mode function of the MKY40 (5 V) which is a CUnet Family Station-IC product. The function and operation of the MKY43 as a CUnet Family-IC are the same as the MEM mode of the MKY40.
For the MKY43, all the CUnet protocol is installed in the hardware, so the user using the CUnet communication is also freed from the complicated processing such as the communications protocol. The CUnet communication is extremely fast and is also protected by a robust test technique, so it can also be used inside the industrial instruments and inside the equipment. Using the MKY43, the CUnet can be used at a lower power consumption and reasonable cost. A "CUnet station" with the MKY43 is called a "MEM station".
The CUnet station with the MKY43 can also be used as a "GMM station" operated by a global memory data monitoring (GMM) function (refer to ***"4.4.8 Global Memory Monitor (GMM) Function"***).

1.1 CUnet Station in MKY43 (MEM Station)

CUnet consists of multiple user equipment with a CUnet IC and a network connecting these equipment. The CUnet IC MKY43 has a bus interface (BUS I/F) and a network interface (network I/F). Connecting the BUS I/F to a CPU and the network I/F to a network offers the user equipment as one MEM station in the CUnet (Fig. 1.1).

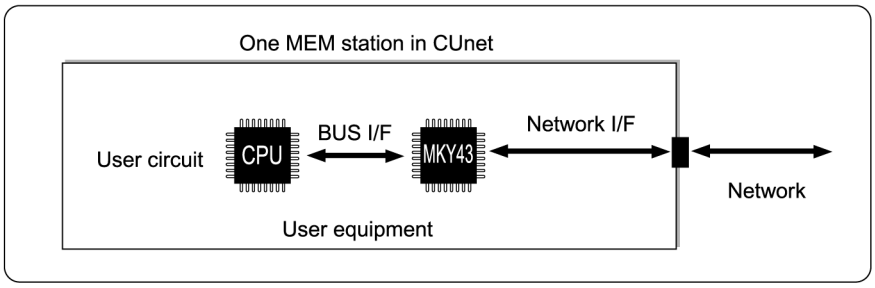


Fig. 1.1 CUnet Station with MKY43 (MEM Station)

The CUnet system shown in Figure 1.2 shares memory data between four MEM stations. The CPU in each MEM station communicates with the others simply and rapidly just by read and write access to a Global Memory (GM) area in the MKY43. The CPUs in each MEM station can also use a mail send buffer and a mail receive buffer of the MKY43 to send up to 256 bytes of dataset to a specified MEM station.

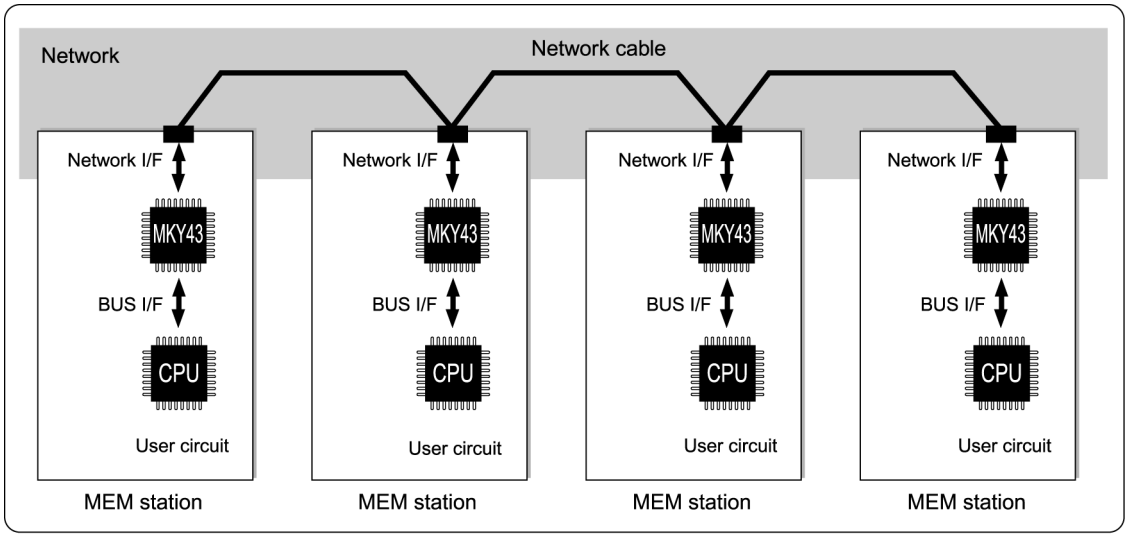


Fig. 1.2 CUnet Connecting Four MEM Stations

1.2 Features of MKY43

The MKY43 has the following features:

(1) Can be connected to up to 64 CUnet stations
(2) 512 bytes of Global Memory (GM) (The memory block size in the CUnet is 8 bytes. GM consists of 64 memory blocks.)
(3) Can own multiple memory blocks
For example, if each MEM station owns 32 memory blocks in the CUnet with two MEM stations, GM can be used as dual-port RAM owning 256 bytes.
(4) Standard baud rates of 12, 6, and 3 Mbps
(5) Can generate various interrupts including ones to detect data transition in GM
(6) Can send a dataset of up to 256 bytes
(7) Can be connected to 8 and 16-bit bus
(8) The CUnet protocol of the MKY43 guarantees that data can be transferred between CUnet stations without error or garbage

Reference For details of the CUnet protocol and data quality assurance, refer to ***"CUnet Introduction Guide"***.

1.3 Connection to I/O Station

In the CUnet system, the I/O station (Fig. 1.3) with a CUnet I/O, such as the MKY46, can be connected to the network. The connection enables I/O signals in the I/O station to connect directly to Global Memory (GM) of the MKY43 in the MEM station.

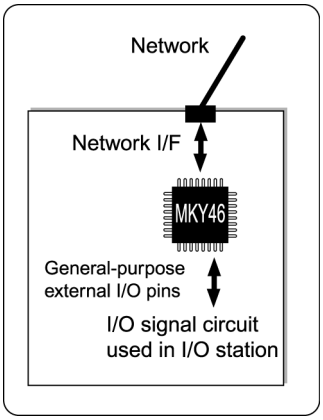


Fig. 1.3 I/O Station

The CUnet system shown in Figure 1.4 is a CUnet that connects two MEM stations with a CPU and the MKY43, and two I/O stations with a CUnet I/O IC, such as the MKY46, via a network.
In this setup, all CPUs can read the state of input ports of the I/O stations from GM of the MKY43. CPUs can also set the state of output ports of the I/O stations by writing data to GM of the MKY43.

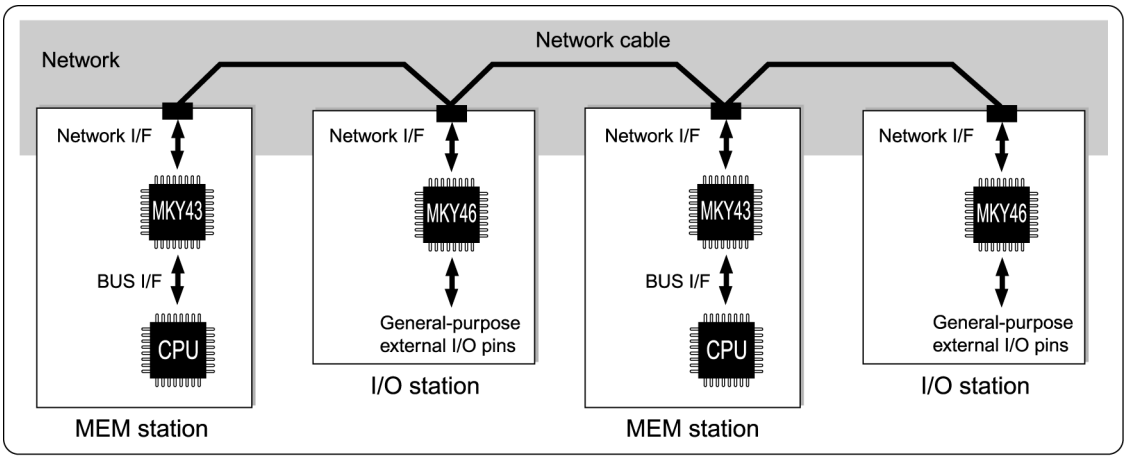


Fig. 1.4 CUnet Connecting I/O Station

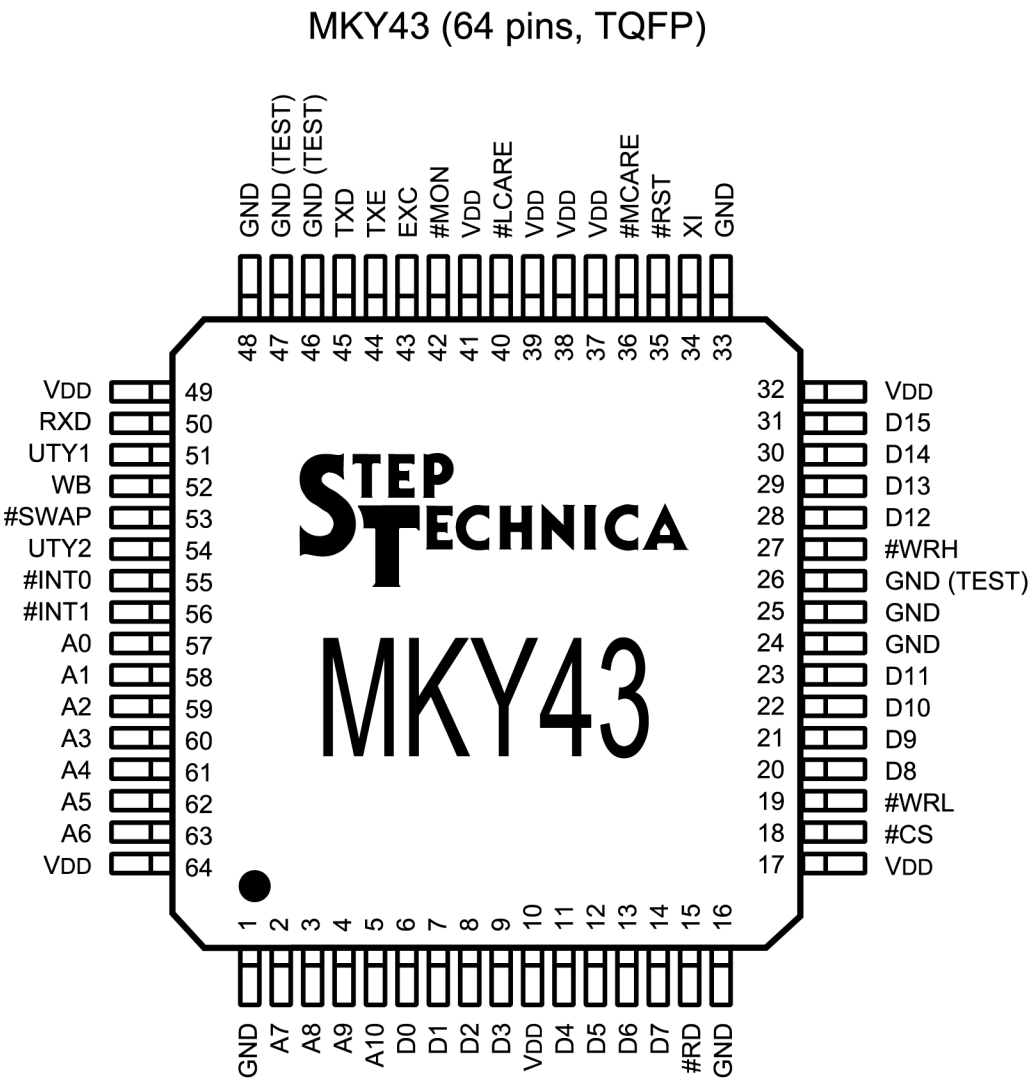
Chapter 2 MKY43 Hardware

This chapter describes the MKY43 hardware, such as pin assignment, pin functions, and I/O circuit types.

Chapter 2 MKY43 Hardware

This chapter describes the MKY43 hardware, such as pin assignment, pin functions, and I/O circuit types.

Figure 2.1 shows the MKY43 pin assignment.



Note: Pins prefixed with # are negative logic (active Low).

Fig. 2.1 MKY43 Pin Assignment

Table 2-1 lists the pin functions of the MKY43.

Table 2-1 Pin Functions of MKY43

Pin name	Pin No.	Logic	I/O	Function
A0 to A10	57 to 63 2 to 5	Positive	I	11-bit address bus that connects to the user bus The A0 pin corresponds to the LSB; the A10 pin corresponds to the MSB. When accessing the MKY43 from the user bus, the signal of these pins must be stabilized before the access condition for the #CS, #RD, #WRH, and #WRL pins is established.
D0 to D15	6 to 9 11 to 14 20 to 23 28 to 31	Positive	I/O	16-bit bidirectional data bus that connects to the user bus The D0 pin corresponds to the LSB; the D15 pin corresponds to the MSB.
#RD	15	Negative	I	Read control pin connected to use bus Set this pin Low at the right time when reading the MKY43. When the WB pin is High and both the #CS and the #RD pins are Low, internal data is output to the 16-bit data bus (D0 to D15). When the WB pin is Low and both the #CS and the #RD pins are Low, internal data is output to the 8-bit data bus (D0 to D7).
#CS	18	Negative	I	Access control pin connected to user bus Set this pin Low at the right time when performing read or write access to the MKY43.
#WRL	19	Negative	I	Write control pin connected to user bus Set this pin Low at the right time when writing to the MKY43. When the WB pin is set to High and when the signal of this pin and the signal of the #WRH pin and #CS pin are all Low, if any of the pins goes High, data in the D0 to D15 bus is written into the MKY43. When the WB pin is set to Low and when both the signals of this pin and the #CS pin are Low, if either of the pins goes High, data in the D0 to D7 bus is written into the MKY43.
#WRH	27	Negative	I	Write control pin to connect to the user bus when the WB pin is set to High Set this pin Low at the right time when writing to the MKY43. When the signal of this pin and the signal of the #WRL pin and #CS pin are all Low, if any of the pins goes High, data in the D0 to D15 bus is written into the MKY43.
Xi	34	Positive	I	Driving clock input pin (48 MHz is recommended)
#RST	35	Negative	I	Input pin for hardware reset of MKY43 Immediately after the power is turned ON or when the user resets hardware intentionally, keep this pin Low for 10 or more clocks of the driving clock.
#MCARE	36	Negative	O	Output pin that outputs Low level for lighting LED for given time at MCARE signal For details when the #MCARE pin goes Low, refer to ***"4.4.5 Controling and Monitoring Network Quality"***.
#LCARE	40	Negative	O	Output pin that outputs Low level for lighting LED for given time at LCARE signal For details when the #LCARE pin goes Low, refer to ***"4.4.5 Controling and Monitoring Network Quality"***.

(Continue)

Table 2-1 Pin Functions of MKY43

(Continued)

Pin name	Pin No.	Logic	I/O	Function
#MON	42	Negative	O	Output pin that outputs Low level for lighting LED while stable link with another CUnet station is established For details when the #MON pin goes Low, refer to ***"4.4.5 Controlling and Monitoring Network Quality"***.
EXC	43	Positive	I	Clock input pin that is used as baud rate depends on external clock The baud rate is 1/4 of the supply frequency, which can be up to 12.5 MHz. Set this pin to High or leave it open when it is not used.
TXE	44	Positive	O	Output pin that goes High during packet output Connect this pin to the enable input pin of the driver.
TXD	45	Positive	O	Output pin that outputs packets Connect this pin to the drive input pin of the driver, etc.
RXD	50	Positive	I	Input pin that inputs packets Connect this pin to the receiver output pin.
UTY1	51	---	Z/O	Pin, which is pulled up internally, that outputs utility signal 1. This pin is kept in the high impedance state pulled up internally, by a hardware reset.
WB	52	Positive	I	Input pin that selects width of bus connected to user bus Set this pin to Low when connecting it to an 8-bit wide user bus. Set this pin to High or leave it open when connecting it to a 16-bit wide user bus.
#SWAP	53	Negative	I	Input pin that selects whether to reverse signal input from A0 pin in MKY43 Set this pin to Low when connecting it to a big-endian type user bus. Set this pin to High or leave it open when connecting it to a little-endian type user bus.
UTY2	54	---	Z/O	Pin, which is pulled up internally, that outputs utility signal 2. This pin is kept in the high impedance state pulled up internally, by a hardware reset.
#INT0	55	Negative	O	Pin that outputs interrupt trigger signals to user bus This pin outputs a Low level when an interrupt trigger occurs.
#INT1	56			
V_{DD}	10, 17, 32, 37, 38, 39, 41, 49, 64	---	---	Power pins for 3.3-V supply
GND	1, 16, 24, 25, 33, 48	---	---	Power pins connected to 0 V
GND (TEST)	26, 46, 47	---	---	Always connect this pin to GND (test pin for manufacturer)

Note: Pins prefixed with # are negative logic (active Low).

Table 2-2 shows the electrical ratings of the MKY43.

Table 2-2 Electrical Ratings of MKY43

(#: Negative logic)

No	I/O	Name	Type	No	I/O	Name	Type	No	I/O	Name	Type	No	I/O	Name	Type
1	--	GND	--	17	--	VDD	--	33	--	GND	--	49	--	VDD	--
2	I	A7	A	18	I	#CS	A	34	I	Xi	A	50	I	RXD	B
3	I	A8	A	19	I	#WRL	A	35	I	#RST	B	51	Z/O	UTY1	F
4	I	A9	A	20	I/O	D8	E	36	O	#MCARE	C	52	I	WB	B
5	I	A10	A	21	I/O	D9	E	37	--	VDD	--	53	I	#SWAP	B
6	I/O	D0	E	22	I/O	D10	E	38	--	VDD	--	54	Z/O	UTY2	F
7	I/O	D1	E	23	I/O	D11	E	39	--	VDD	--	55	O	#INT0	D
8	I/O	D2	E	24	--	GND	--	40	O	#LCARE	C	56	O	#INT1	D
9	I/O	D3	E	25	--	GND	--	41	--	VDD	--	57	I	A0	A
10	--	VDD	--	26	--	GND (TEST)	--	42	O	#MON	C	58	I	A1	A
11	I/O	D4	E	27	I	#WRH	A	43	I	EXC	B	59	I	A2	A
12	I/O	D5	E	28	I/O	D12	E	44	O	TXE	C	60	I	A3	A
13	I/O	D6	E	29	I/O	D13	E	45	O	TXD	C	61	I	A4	A
14	I/O	D7	E	30	I/O	D14	E	46	--	GND (TEST)	--	62	I	A5	A
15	I	#RD	A	31	I/O	D15	E	47	--	GND (TEST)	--	63	I	A6	A
16	--	GND	--	32	--	VDD	--	48	--	GND	--	64	--	VDD	--

Figure 2.2 shows the pin electrical characteristics in I/O circuit types in MKY43.

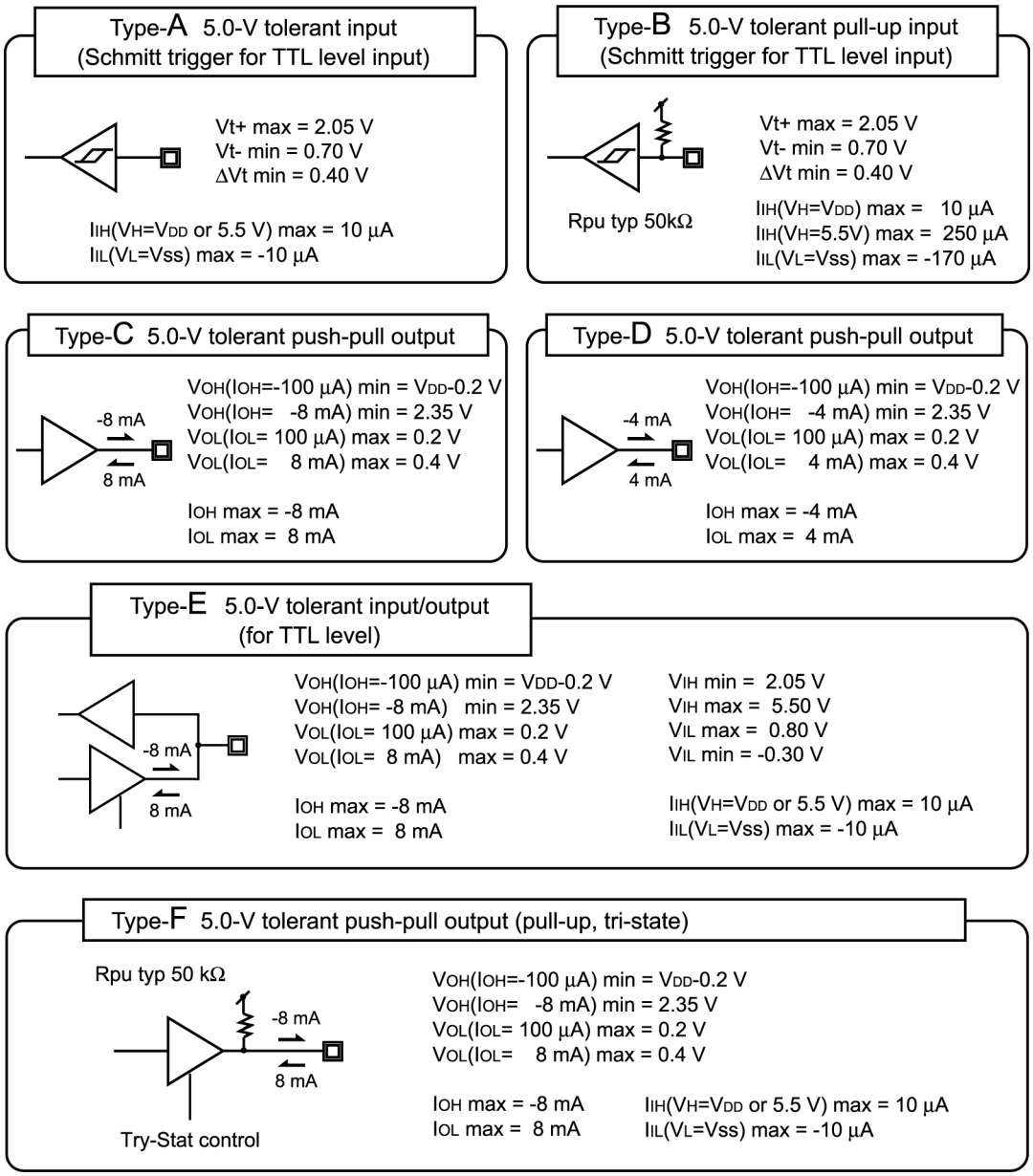

Type-A 5.0-V tolerant input
(Schmitt trigger for TTL level input)
Vt+ max = 2.05 V
Vt- min = 0.70 V
ΔVt min = 0.40 V
IIH(VH=VDD or 5.5 V) max = 10 μA
IIL(VL=Vss) max = -10 μA
Type-B 5.0-V tolerant pull-up input
(Schmitt trigger for TTL level input)
Vt+ max = 2.05 V
Vt- min = 0.70 V
ΔVt min = 0.40 V
Rpu typ 50kΩ
IIH(VH=VDD) max = 10 μA
IIH(VH=5.5V) max = 250 μA
IIL(VL=Vss) max = -170 μA
Type-C 5.0-V tolerant push-pull output
-8 mA
8 mA
VOH(IOH=-100 μA) min = VDD-0.2 V
VOH(IOH= -8 mA) min = 2.35 V
VOL(IOL= 100 μA) max = 0.2 V
VOL(IOL= 8 mA) max = 0.4 V
IOH max = -8 mA
IOL max = 8 mA
Type-D 5.0-V tolerant push-pull output
-4 mA
4 mA
VOH(IOH=-100 μA) min = VDD-0.2 V
VOH(IOH= -4 mA) min = 2.35 V
VOL(IOL= 100 μA) max = 0.2 V
VOL(IOL= 4 mA) max = 0.4 V
IOH max = -4 mA
IOL max = 4 mA
Type-E 5.0-V tolerant input/output
(for TTL level)
-8 mA
8 mA
VOH(IOH=-100 μA) min = VDD-0.2 V
VOH(IOH= -8 mA) min = 2.35 V
VOL(IOL= 100 μA) max = 0.2 V
VOL(IOL= 8 mA) max = 0.4 V
IOH max = -8 mA
IOL max = 8 mA
VIH min = 2.05 V
VIH max = 5.50 V
VIL max = 0.80 V
VIL min = -0.30 V
IIH(VH=VDD or 5.5 V) max = 10 μA
IIL(VL=Vss) max = -10 μA
Type-F 5.0-V tolerant push-pull output (pull-up, tri-state)
Rpu typ 50 kΩ
-8 mA
8 mA
Try-Stat control
VOH(IOH=-100 μA) min = VDD-0.2 V
VOH(IOH= -8 mA) min = 2.35 V
VOL(IOL= 100 μA) max = 0.2 V
VOL(IOL= 8 mA) max = 0.4 V
IOH max = -8 mA
IOL max = 8 mA
IIH(VH=VDD or 5.5 V) max = 10 μA
IIL(VL=Vss) max = -10 μA

Fig. 2.2 Pin Electrical Characteristics in I/O Circuit Types of MKY43

Chapter 3 Connecting MKY43

This chapter describes the pin functions and connections required for the MKY43 to function.

3.1 Voltage Levels of Pins Connecting to Signal Pins.....3-4
3.2 Supplying Driving Clock and Hardware Reset Signal.....3-6
3.3 Connecting Network Interface.....3-7
3.4 Setting Baud Rate.....3-8
3.5 Network Cable Length.....3-9
3.6 Setting Station Addresses and Owned Area.....3-10
3.7 Connecting LED Indication Pins.....3-10
3.8 Connection of UTY1 Pin and UTY2 Pin.....3-11
3.9 Connecting User Bus.....3-13

Chapter 3 Connecting MKY43

This chapter describes the pin functions and connections required for the MKY43 to function.

When connecting the MKY43, be sure to connect the GND (TEST) pins (pins 26, 47, 48) to the GND pins. Be sure to connect all the V_{DD} pins (pins 10, 17, 32, 37, 38, 39, 41, 49, 64) to the 3.3-V power supply, and all the GND pins (pins 1, 16, 24, 25, 33, 48) to the 0-V power supply. In addition, connect a capacitor of 10 V/0.1 μF (104) or more between adjacent V_{DD} pins and GND pins.

3.1 Voltage Levels of Pins Connecting to Signal Pins

All the signal pins except those connected to VDD pins or GND pins of the MKY43 are tolerant pins that can be connected to 5.0-V TTL signals.

This enables pins to be connected to the CPU and peripheral logic circuit driven by 3.3-V and 5.0-V power supplies.

(1) The pins can directly be connected to the CPU and peripheral logic circuit driven by the 3.3-V power supply.

(2) The pins can be connected to TTL-level signals of the CPU and peripheral logic circuit driven by the 5.0-V power supply. A pull-up resistor can also be connected between 5.0-V power supplies. However, if the input voltage of the MKY43 pins exceeds 3.3 V, leakage current flows into the MKY43 pins (Fig. 3.1).

(3) Because the High-level voltage does not meet the 5.0-V CMOS input specifications, the MKY43 output pins cannot be connected to the CMOS input pins of the CPU and peripheral logic circuit driven by the 5.0-V power supply. The pins cannot be connected even if a pull-up resistor is used between the 5.0-V power supplies (Fig. 3.1).

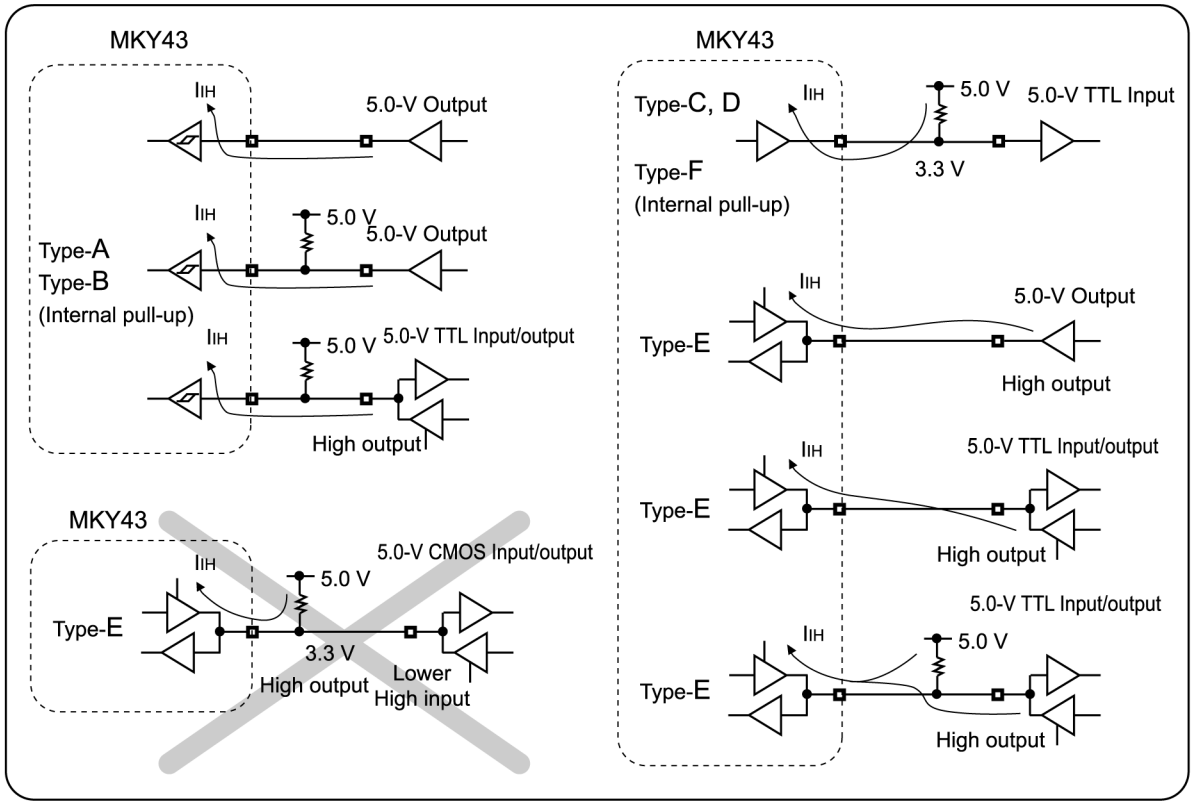


Fig. 3.1 Connection Causing Leakage Current

Caution

(1) When signal connecting to LSIs with different power-supply voltages, be sure to check the input/output electric specifications for the LSIs to connect. Also, a voltage must not stay supplied to signal pins when the MKY43 is power-off.

(2) In the MKY43, if an external pull-up resistor is connected between non-pull-up input pins and high-impedance pins and the 5.0-V power supply, the voltage level is increased up to 5.0 V. Depending on the circuit conditions on the circuit board with the MKY43, several tens of μs to several ms may be required to increase the voltage level. StepTechnica recommends pull-up resistors of 3 to 30 kΩ be connected.

(3) A pull-up resistor can be connected between the MKY43 output pins and the 5.0-V power supply. In this case, the High-level output is increased up to 3.3 V, but not to 5.0 V (Fig. 3.1).

3.2 Supplying Driving Clock and Hardware Reset Signal

This section describes how to supply a clock that drives the MKY43 and a hardware reset signal.

3.2.1 Supply of Driving Clock

Connect an oscillator-generated clock to the Xi pin (pin 34) of the MKY43 for driving clock in accordance with the follwing specifications. The MKY43 executes all operations using the clock signal supplied to the Xi pin. If a clock signal is not supplied, the user system program does not have read and write access to the MKY43 memory.

(1) Usually supply a 48 MHz external clock. The upper frequency is 50 MHz, and the lower frequency is not provided
(2) Electrical characteristics of the Xi pin: V_{IH} = min 2.05 V, V_{IL} = max 0.70 V
(3) Clock with a signal rise and fall time of 20 ns or less
(4) Clock with a minimum High-level or Low-level time of 5 ns or more
(5) Connect a clock with jitter component of:
- 250 ps or less at input frequency of 25 MHz or more
- 500 ps or less at input frequency of less than 25 MHz

(6) Connect a clock with a frequency accuracy of ±500 ppm or better.

Reference For a commonly-used oscillator, there is no problem with clock output by the values above in (2) to (6).

3.2.2 Supply of Hardware Reset Signal

When a Low level signal is supplied to the #RST (ReSeT) pin (pin 35), the MKY43 is hardware-reset. If a period in which the Low-level signal has been supplied is less than "one clock", the signal is ignored to prevent malfunction. To reset the MKY43 completely, the #RST pin must be kept Low for "10 or more clock" while supplying a driving clock (Fig. 3.2).

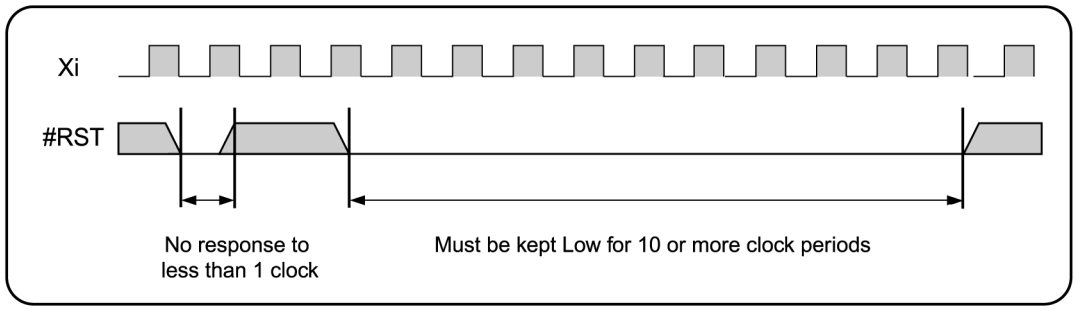


Fig. 3.2 Hardware Reset

Caution Design the circuit so that a hardware reset is surely activated immediately after MKY43 power-on.

3.3 Connecting Network Interface

The network interface (network I/F) pins of the MKY43 consist of RXD (pin 50), TXE (pin 44), and TXD (pin 45).

3.3.1 Recommended Network Connection

Figure 3.3 shows the recommended network connection. The TRX (driver/receiver components) consists of an RS-485-based driver/receiver and a pulse transformer. Recommended network cables include Ethernet LAN cable (10BASE-T, Category 3 or higher) and shielded network cables. Use one twisted-pair cable in the network cable.

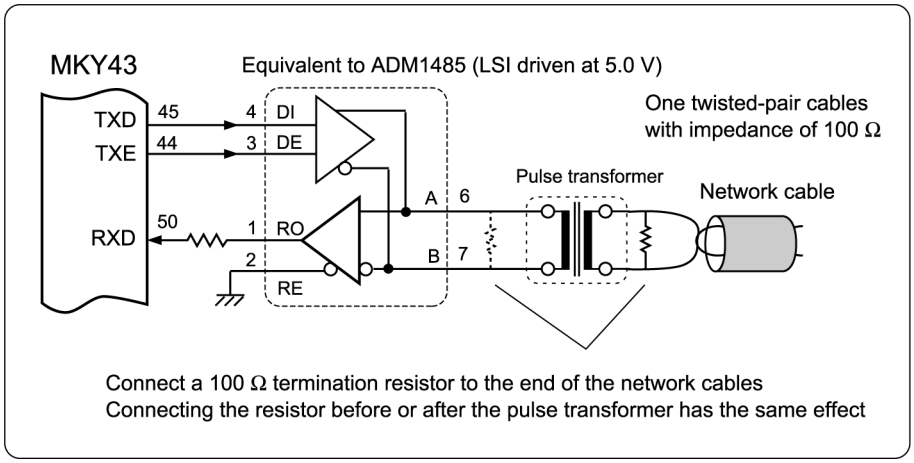


Fig. 3.3 Recommended Network Connection

Reference

Depending on the TRX configuration in half-duplex mode, signals output from the TXD pin may be output directly to the RXD pin while the MKY43 transmits packets. However, the MKY43 is designed not to receive any packet transmitted by itself while the TXE pin is High, so there is no problem.

Background information to help build a network are described in ***"CUnet Technical Guide"***. For more information about how to select components or to get recommended components, visit our Web site at **www.steptechnica.com/**.

3.3.2 Details of RXD, TXE, and TXD Pins

The MKY43 receives packets transmitted from another CUnet station at the RXD pin and outputs packets transmitted to another CUnet station from the TXD pin. During sending a packet, a High level is output from the TXE pin. When the TXE pin goes High, design the TRX so that the enable pin of the TRX driver is activated, thereby enabling the serial pattern for a packet output from the TXD pin to be transmitted to the network (Fig. 3.3).

3.4 Setting Baud Rate

To set the baud rate of the MKY43, use bit 7 (BPS1) and bit 6 (BPS0) of the Basic Control Register (BCR). For details, refer to ***"4.1.3 Initialization and Start-up of Communication"***.

When "00B" is set as the baud rate, the baud rate is "1/4" of the clock frequency supplied to the EXC pin (pin 43). (For example, when the clock frequency supplied to the EXC pin is 5 MHz, the baud rate is 1.25 Mbps.) The maximum clock frequency that can be supplied to the EXC pin is 12.5 MHz with a duty ratio ranging from 40% to 60% (when Xi = 50 MHz). When not supplying a clock frequency to the EXC pin, leave the EXC pin open or connect it to VDD or GND because the EXC pin is connected pull-up resistor internally.

(1) Set the same baud rates to all CUnet devices connected to the network.
(2) In the state in which the clock is not supplied to the EXC pin, if the BPS of the BCR is set to "00B" (the EXC is selected), the communications system inside the MKY43 does not operate.
(3) Our recommended pulse transformers may not support baud rates other than "12 Mbps to 3 Mbps". In this case, use a pulse transformer matching the baud rate.

3.5 Network Cable Length

In this manual, each connection point of a multi-drop network cable is called a “branch”.
Table 3-1 indicates the network cable length for the CUnet when using the network described in ***“3.3 Connecting Network Interface”*** with 32 or less branches.

Table 3-1 Network Cable Length

Baud rate	Network cable length
12 Mbps	100 m
6 Mbps	200 m
3 Mbps	300 m

The recommended differential driver/receiver is an RS-485-based driver/receiver. Therefore, the branch count “32” stipulated in the RS-485 specification is used as a guide in Table 3-1.
Up to 64 CUnet stations can be connected to the CUnet, enabling connection of “64” branches. This recommended network is isolated electrically by a pulse transformer and the format of signals propagated through the network is RZ (Return to Zero). Consequently, “64” branches can be connected using a standard RS-485-based driver/receiver without using DC component signals. In this case, the cable length is likely to be shorter than the value in Table 3-1 (due to increase of dispersion of propagated signal energy).

Before using a CUnet, perform function tests in the use environment and confirm that CUnet operation is stable without LCARE (Link CARE) and MCARE (Member CARE) described in ***“4.4.5 Controling and Monitoring Network Quality”***.

Network cable length can be extended by setting the frame option or adding HUB(s). For detail, refer to ***“4.4.9 Frame Option [for HUB]”*** and ***“User’s Manual”*** for ***“HUB-IC MKY02”***.

The network cable length varies depending on the cable quality, differential driver/receiver components, cable connection status, and environment. Therefore, values in ***“Table 3-1 Network Cable Length”*** are only a guide and performance is not guaranteed.

3.6 Setting Station Addresses and Owned Area

For the MKY43, the Station Address (SA), the block count of owned width (OWN width: "00H to 3FH"), and the baud rate (the BPS bit) are set by using the Basic Control (BCR). For details, refer to ***"4.1.3 Initialization and Start-up of Communication"***.

Caution The same SA values cannot be set to all CUnet ICs connected to one network. Duplication of owned areas by expansion setting is prohibited.

3.7 Connecting LED Indication Pins

The MKY43 has three output pins for LED indication, #MON (pin 42), #LCARE (pin 40), and #MCARE (pin 36), each of which outputs active-Low signals (Low level at active).

These pins can drive a current of ±8 mA. If LEDs can be turned on at a current of 8 mA or less, they can be connected to go on at a Low level (Fig. 3.4). The user system hardware designer should determine the value of each current-limiting resistor in Figure 3.4 according to the LED ratings.

The green LED indicating stable operation should be connected to the #MON pin and the orange LED indicating medium-level warning should be connected to the #LCARE pin. The red LED indicating a clear warning should be connected to the #MCARE pin. For details when the #MON, #LCARE, and #MCARE pins go Low, refer to ***"4.4.5 Controling and Monitoring Network Quality"***. Leave the #MON, #LCARE, and #MCARE pins open when they are not used.

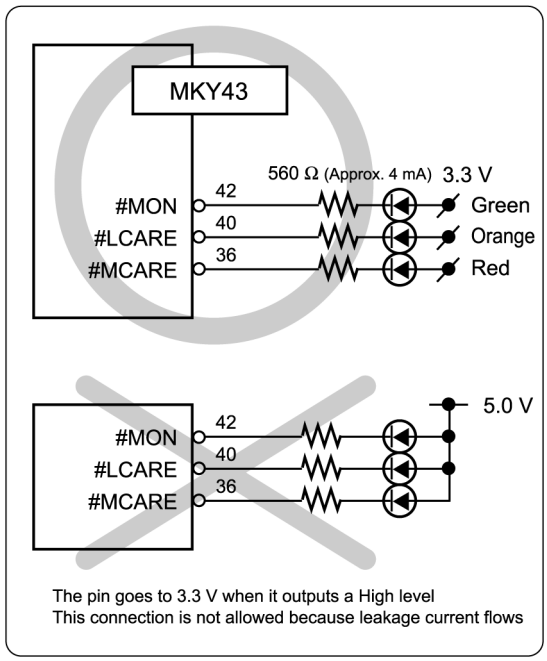


Fig. 3.4 LED Connection

Caution When the anode side of the LED is connected to the 5.0-V power supply, as shown in Figure 3.4, the LED may go on due to the leakage current. Do not perform such a connection.

3.8 Connection of UTY1 Pin and UTY2 Pin

The MKY43 has the #CYCT output signal to notify the start timing of the cycle, and the #PING output signal to notify the reception of the PING instruction from another CUnet station. These two signals can be output to the UTY1 (UTilitY 1) pin (pin 51) or UTY2 (UTilitY 2) pin (pin 54) by setting the UTCR (UTility pin Control Register).

When a hardware reset is activated, the UTY1 pin and UTY2 pin are kept in the high impedance state pulled up internally. Leave the UTY1 pin and UTY2 pin open when not used (Fig. 3.5).

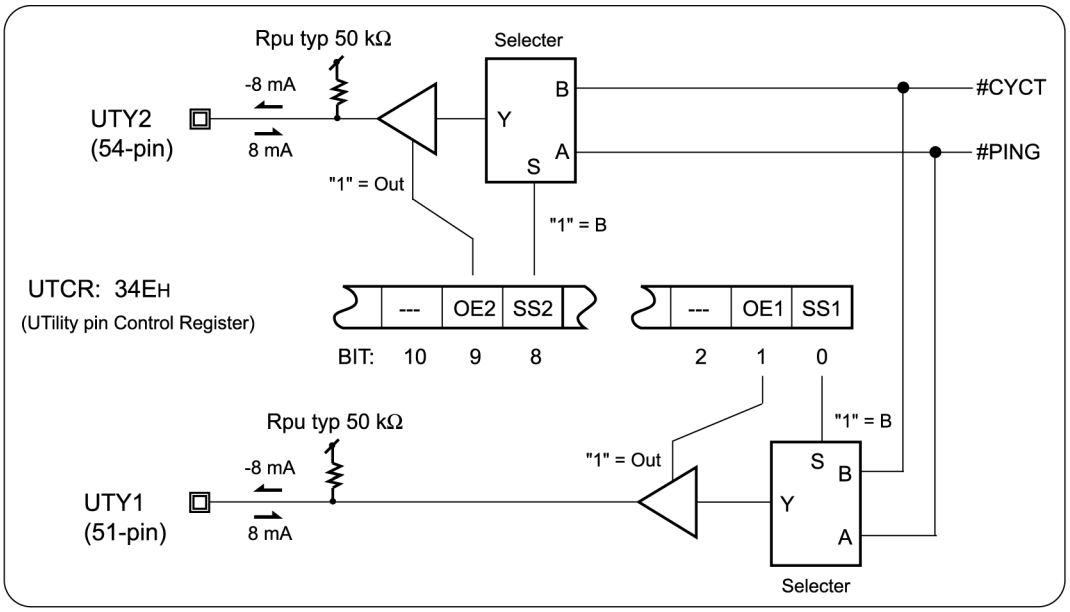


Fig. 3.5 UTY1 Pin and UTY2 Pin Control

3.8.1 Details of #CYCT Signal

The pin to which the #CYCT signal output is selected is usually kept High and outputs a pulse that goes Low for "2 × TBPS" time at the start timing for a cycle. Using the timing at which the output of this pin changes to Low allows the user to recognize the timing (synchronization) common to all CUnet stations connected to a network.
The synchronous performance of a CUnet can be calculated using equation 3.1.

Equation 3.1 (2 × TBPS) + (cycle time × clock accuracy) + signal propagation delay [or less]

For example, the synchronous performance is calculated as follows at 12 Mbps (TBPS = 83.3 ns), with 64 CUnet stations (cycle time = 2.365 ms), at a driving clock accuracy of 200 ppm (0.02%) and a total length of cable (7 ns/m) of 100 m:
(167 ns + 473 ns + 700 ns) ≈ 1.34 μs max.

This equation cannot be used when a HUB is inserted into a network.

(1) The #CYCT signal in the MKY43 is the same as the #STB signal in the MKY40.
(2) Referencing the SCR and receiving interrupt triggers enables a user system program running on a CPU to recognize the cycle timing (refer to ***"4.1.7 Detailed Timing during Cycle"*** and ***"4.5 Interrupt Trigger Generation Function"***). However, in this case, the timing accuracy depends on the program running status. By comparison, the output signal of the pin serves many uses mainly in supplying high-accuracy synchronization signals to peripheral user circuits.

3.8.2 Details of #PING Signal

The #PING signal is operated by another CUnet station, regardless of the self-station state.
The pin to which the #PING signal output is selected is usually kept High. The pin changes to Low at receipt of the PING instruction from another CUnet station. The pin then changes to High at receipt of packets from another CUnet station that do not contain the PING instruction.
The CUnet protocol does not define why to use and where to connect the PING signal. The #PING signal is an auxiliary expanded function to support creation of a user application.
For details about how to generate a #PING signal, refer to ***"4.4.6 PING Instruction"***.

"Forcibly resetting a CPU from a network" can be an example of using the #PING signal. For example, if a program for a CPU with the CUnet station runs away, it can be reset from another CUnet station (if the output of the #PING signal can perform a hardware reset).

3.9 Connecting User Bus

This section describes how to connect the CPU and access time necessary for access to the MKY43 from the user system program. In this section, the bus signals such as address and data including control signals such as chip select (CS), read (RD) and write (WR) output directly from the CPU, are collectivelly called the "user bus". Signals traveling via a bus driver or bus controller are also called the user bus.

3.9.1 Data Storage Method

To optimize word access with the 16-bit bus, the 16-bit register of the MKY43 is aligned on 2-byte boundaries and the 64-bit register of the MKY43 is aligned on 8-byte boundaries.
When using byte access with the 16-bit bus, register addresses vary depending on the endian type of the user bus. Figure 3.6 shows an example of reading the same register with a big-endian user bus and a little-endian user bus. When the MKY43 is connected with the 16-bit bus, StepTechnica recommends word access be used to access, except that the user system program uses byte access after it identifies differences between register addresses.

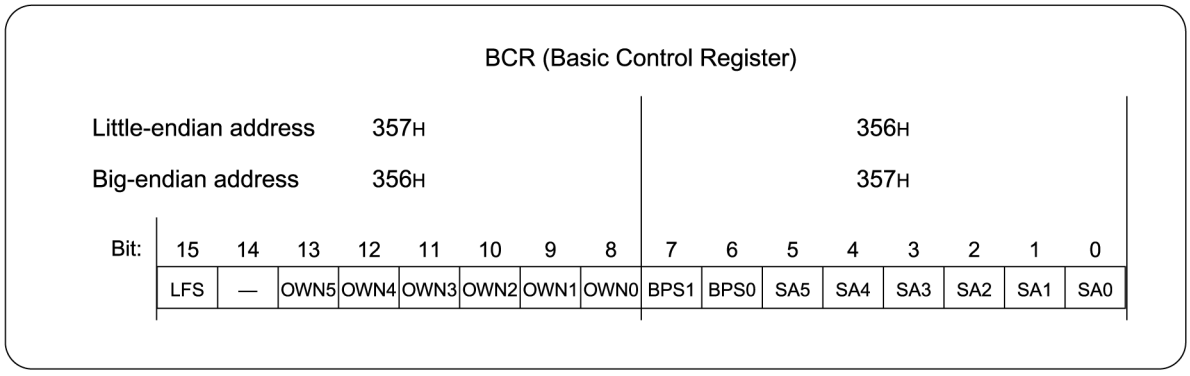

BCR (Basic Control Register)
Little-endian address
357H
356H
Big-endian address
356H
357H
Bit:
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
LFS — OWN5 OWN4 OWN3 OWN2 OWN1 OWN0 BPS1 BPS0 SA5 SA4 SA3 SA2 SA1 SA0

Fig. 3.6 Differences between Addresses for Byte Access Depending on Endian

3.9.2 Function of #SWAP Pin

When connecting an 8-bit user bus, the MKY43 has a function (#SWAP pin) to absorb the above address differences.
When the #SWAP pin is Low, the MKY43 inverts a signal level input to the A0 pin internally recognizes the level. When the #SWAP pin is Low and an 8-bit and big-endian user bus indicates address 000H, the MKY43 recognizes "address 001H". When the user bus indicates address 001H, the MKY43 recognizes it "address 000H". The #SWAP pin allows the MKY43 to identify the address signal A0 of the big-endian user bus with that of the little-endian user bus.

Caution When using byte access in the MKY43 connected with a 16-bit bus, the #SWAP pin doesn't function due to a logic circuit, i.e. it cannot absorb the address differences caused by endian (This is because the significance of the address signal A0). In the MKY43 connected with a 16-bit wide bus, StepTechnica recommends word access be used to access.

3.9.3 Connection to 16-bit User Bus

This section describes how to connect the MKY43 to a 16-bit user bus (Fig. 3.7).

(1) Set the WB pin (pin 52) of the MKY43 High level (or leave it open).

(2) Connect address signals A1 to A10 of the user bus to the A1 to A10 pins (pins 58 to 63 and pins 2 to 5) of the MKY43. The A0 pin (pin 57) of the MKY43 is not used. The A0 pin is an input pin, and connect a pull-up or pull-down resistor of about 30 kΩ to the A0 pin or connect to VDD or GND, or to the address signal A0 of the user bus to prevent the A0 pin from being input an undefined level.

(3) The #SWAP pin (pin 53) of the MKY43 does not function in the MKY43 connected with 16-bit wide bus. It is an internally pulled-up input pin, so leave the #SWAP pin open or connect it to VDD.

(4) Connect data signals D0 to D15 of the user bus to the D0 to D15 pins (pins 6 to 9, pins 11 to 14, pins 20 to 23, and pins 28 to 31) of the MKY43.

(5) Connect the RD signal of the user bus to the #RD pin (pin 15) of the MKY43, the WRH signal to the #WRH pin (pin 27), and the WRL signal to the #WRL pin (pin 19). When the #CS pin (pin 18) of the MKY43 is Low, the RD, WRH, and WRL signals of the user bus are activated. Also, if only one WR signal of the user bus is present, connect that WR signal to both the #WRH pin and #WRL pin of the MKY43.

(6) Connect the signal that the user bus generates to determine the memory, allocation of the MKY43, to the #CS pin (pin 18) of the MKY43. The #CS input pin functions when Low.

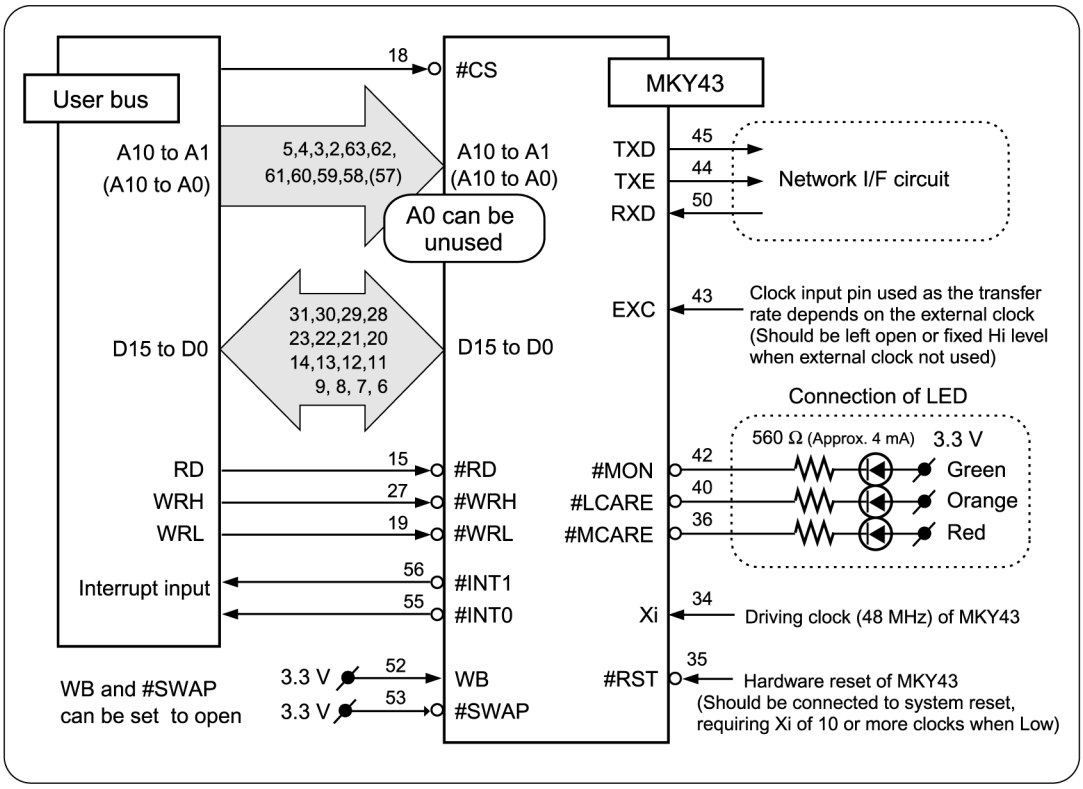


Fig. 3.7 Connection to 16-bit User Bus

3.9.4 Connection to 8-bit User Bus

This section describes how to connect the MKY43 to an 8-bit user bus (Fig. 3.8).

(1) Set the WB pin (pin 52) of the MKY43 Low level.

(2) Connect address signals A0 to A10 of the user bus to the A0 to A10 pins (pins 57 to 63 and pins 2 to 5) of the MKY43.

(3) For a big-endian user bus, set the #SWAP pin (pin 53) Low level; for a little-endian user bus, set the pin High (or leave it open).

(4) Connect data signals D0 to D7 of the user bus to the D0 to D7 pins (pins 6 to 9 and pins 11 to 14) of the MKY43. Since the D8 to D15 pins (pins 20 to 23 and pins 28 to 31) of the MKY43 are unused input pins, connect a pull-up or a pull-down resistor of about 30 kΩ to these pins or connect to VDD or GND to prevent these pins from being input undefined levels.

(5) Connect the RD signal and the WR signal of the user bus to the #RD pin (pin 15) and the #WRL pin (pin 19) of the MKY43, respectively. When the #CS pin (pin 18) of the MKY43 is Low, the RD signal and WR signal of the user bus are activated.

The #WRH pin of the MKY43 is an input pin, and it is not used in the MKY43 connected with an 8-bit wide bus. Connect a pull-up resistor of about 30 kΩ to the #WPH pin or connect to VDD to prevent the pin from being input an undefined level.

(6) Connect a signal that is generated in the user bus to determine the memory, allocation of the MKY43, to the #CS pin (pin 18) of the MKY43. The #CS input pin functions when it is Low.

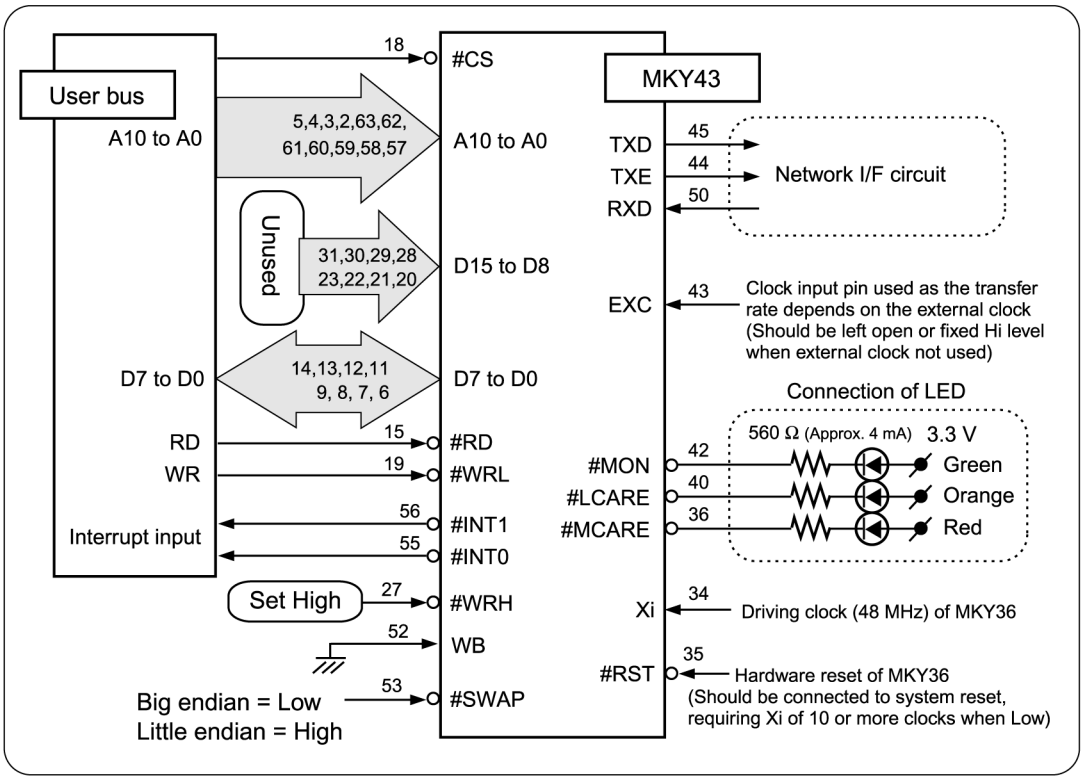


Fig. 3.8 Connection to 8-bit User Bus

3.9.5 Recognition of Access

The conditions for recognizing that the MKY43 is accessed from the user bus are as follows:

(1) Read: When both #CS pin and #RD pin Low, and #WRH pin and #WRL pin High

For example, when only the #RD pin is Low, read access is not started and data is not output to the data bus.

The MKY43 whose WB pin is set to High outputs internal data to the 16-bit data bus from D0 to D15, when both the #CS and the #RD pins are Low.

The MKY43 whose WB pin is set to Low outputs internal data to the 8-bit data bus from D0 to D7, when both the #CS and the #RD pins are Low.

(2) Write: In the case where WB pin is High: When #RD pin High and #CS pin Low, and also both #WRH pin and #WRL pin Low

For example, after all of the #CS pin, #WRH pin, and the #WRL pin are Low and only the #WRH pin goes High, write access is assumed to have been terminated, and 16-bit data on the data bus from D0 to D15 are input.

Write: In the case of Low WB pin: When #WRL pin Low, and #RD pin High and #CS pin Low

For example, after both the #CS pin and #WRL pin are Low and only the #CS pin goes High, write access is assumed to have been terminated, and 8-bit data on the data bus from D0 to D7 are input.

3.9.6 Design of Access Time

For the MKY43 running at 48 MHz, read access requires 89 ns when condition (1) described in ***"3.9.5 Recognition of Access"*** is established and write access requires 63 ns when condition (2) described in ***"3.9.5 Recognition of Access"*** is established. In addition, the MKY43 running at 48 MHz requires an access pause time of 2 TXI (about 43 ns) or more between the following accesses.

(1) Read access after read access
(2) Write access after read access
(3) Read access after write access
(4) Write access after write access

There should be sufficient access time to design connection between the user bus and the MKY43.

For details of the MKY43 timing, refer to ***"6.2 AC Characteristics"***.

3.9.7 Access Tests after Embedding MKY43

For details of how to check addresses and access tests after connecting the MKY43 to the user equipment, refer to ***"4.1.2 Checking for Connection of MKY43"***.

3.9.8 Interrupt Trigger to CPU

The MKY43 has two output pins, #INT0 and #INT1 pins (pins 55 and 56) that supply signals to the interrupt trigger pins of the CPU. The #INT0 and #INT1 pins output High level when a hardware reset is activated and they output a Low level when an interrupt trigger occurs. The Low level of the pin changes from Low to High when the user system program accesses the MKY43 register.

Multiple interrupt factors can be set to the #INT0 and #INT1 pins.
The #INT0 and #INT1 pins have retrigger function. The retrigger function may allow output levels of the #INT0 and #INT1 pins change from High to Low level again after 10 clocks (208 ns for 48-MHz clock) elapse immediately after output level of the #INT0 and #INT1 pins have changed from Low to High level.

To connect #INT0 and #INT1 pins (or either pin) to the interrupt trigger pin of the CPU, follow the specification of the CPU. When not used, leave these pins open.

For details of the #INT0 and #INT1 pins, refer to ***"4.5 Interrupt Trigger Generation Function"***.

Chapter 4 MKY43 Software

This chapter describes the software to use the MKY43. It also assumes that the connection between the user bus and the MKY43 based on the description in ***"Chapter 3 Connecting MKY43"*** allows the user system program to access the MKY43.

4.1 Start and Stop of Communication 4-3
4.2 Use of GM 4-11
4.3 Use of Mail Sending/Reception Function 4-28
4.4 Detailed Operation and Management of CUnet System 4-37
4.5 Interrupt Trigger Generation Function 4-54

Chapter 4 MKY43 Software

This chapter describes the software to use the MKY43. It also assumes that the connection between the user bus and the MKY43 based on the description in ***"Chapter 3 Connecting MKY43"*** allows the user system program to access the MKY43.

4.1 Start and Stop of Communication

This section describes the operation of the MKY43 by the user CPU.

The basic items to operate the MKY43 are described in the following order.

(1) Memory map
(2) Checking for connection of MKY43
(3) Setting (initialization) before communication start to initialization
(4) Responses to each phase
(5) Protection against misoperation
(6) Cycle time of CUnet
(7) Detailed timing during cycle
(8) Network stop

4.1.1 Memory Map

The MKY43 connected to the user CPU occupies "2 KB (2048 bytes: 000H to 7FFH)" of memory area. Table 4-1 shows the memory map.

Table 4-1 Memory Map

Address	Function
000H to 1FFH	Global Memory (GM)
200H to 2FFH	Mail Send Buffer (MSB)
300H to 3FFH	Register and the maker reserve (390H to 3FFH)
400H to 4FFH	Mail Receive Buffer 0 (MRB0)
500H to 5FFH	Mail Receive Buffer 1 (MRB1)
600H to 7FFH	The maker reserve area

Caution Memory and register addresses indicated in the MKY43 memory map are on the 4-byte or 2-byte boundary. If the user CPU performs access to the MKY43 from the 8-bit wide data bus, the lower addresses may differ, depending on the endian type. For details, refer to ***"3.9.1 Data Storage Method"***.

4.1.2 Checking Connection of MKY43

When the MKY43 is connected correctly to the user CPU, the ASCII character string "MKY43_v0" can be read when the Chip Code Register (CCR) is read. If this character string can be read, the user CPU can check that the MKY43 is connected. The character string is "MKY43_v0" when read from a little-endian user CPU, and the array of the characters differs when read from a big-endian user CPU.
When the network is not started (the START bit of the SCR (System Control Register) is "0"), any data can be written to all memory, except registers (300H to 3FFH) and the maker reserve area (600H to 7FFH) of the MKY43. When any data is written to each memory for read verification, the user CPU can check that the MKY43 is correctly connected to the user CPU.

4.1.3 Initialization and Start-up of Communication

This section describes how to start communication (Fig. 4.1).

(1) Memory in the MKY43 after power-on contains undefined values. Clear the undefined values by writing data of value "00H" to memory (GM, MSB, MRB0, MRB1) except the register area at addresses 300H to 3FFH (Table 4-1).

(2) Set the Station Address (SA), OWN width (OWN), and baud rate (BPS) to the BCR (Basic Control Register). To prevent accidental writing during network operation, the BCR can be written only when bit 15 (GMM) of the SCR (System Control Register) is "1". To write setting values to the BCR using the user system program, follow the procedure below:

1. Check that bit 8 (START) of the SCR is "0".
2. Write "1" to bit 15 (GMM) of the SCR.
3. Write the SA values to bits 0 to 5 (SA0 to SA5) of the BCR, the baud rate values to bits 6 and 7 (BPS0 and BPS1), and the OWN width (OWN) values to bits 8 to 13 (OWN0 to OWN5). Normally, write "0" to LFS (Long Frame Select) of bit 15 (refer to ***"4.4.9 Frame Option [for HUB]"***).
4. Write "0" to bit 15 (GMM) of the SCR.

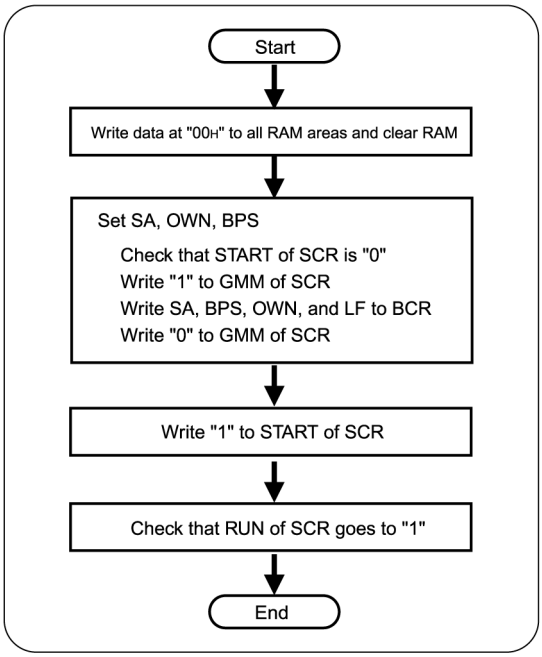

Start
Write data at "00H" to all RAM areas and clear RAM
Set SA, OWN, BPS
Check that START of SCR is "0"
Write "1" to GMM of SCR
Write SA, BPS, OWN, and LF to BCR
Write "0" to GMM of SCR
Write "1" to START of SCR
Check that RUN of SCR goes to "1"
End

Fig. 4.1 Start Algorithm

(3) Write "1" to bit 8 (START) of the SCR. The CUnet network starts and the MKY43 enters the START phase.

(4) Read the SCR to check that bit 9 (RUN) is "1" (, which means the MKY43 enters the RUN phase). If bit 9 (RUN) of the SCR does not go to "1" and bit 10 (CALL) or bit 11 (BRK) goes to "1" (when the MKY43 is in any phase other than RUN), follow the description in ***"4.1.4 Responses to Each Phase"***.

(5) When bit 9 (RUN) of the SCR is "1", the user system can use "sharing memory data using GM" and "CUnet communication by mail sending/receiving of datasets using the mail send buffer and mail receive buffer".

Reference When the RUN flag bit goes to "1" (when the MKY43 enters the RUN phase), the MKY43 can output interrupt triggers. For details, refer to ***"4.5 Interrupt Trigger Generation Function"***.

4.1.4 Responses to Each Phase

The MKY43 changes to any of the CALL phase, RUN phase, or BREAK phase in 2 or 3 cycles in the START phase after the network is started in accordance with the phase transition defined in the CUnet protocol. Each phase of the MKY43, indicated by the RUN, CALL, and BRK bits of the SCR (System Control Register) can be recognized by reading the SCR using the user system program (Fig. 4.2).

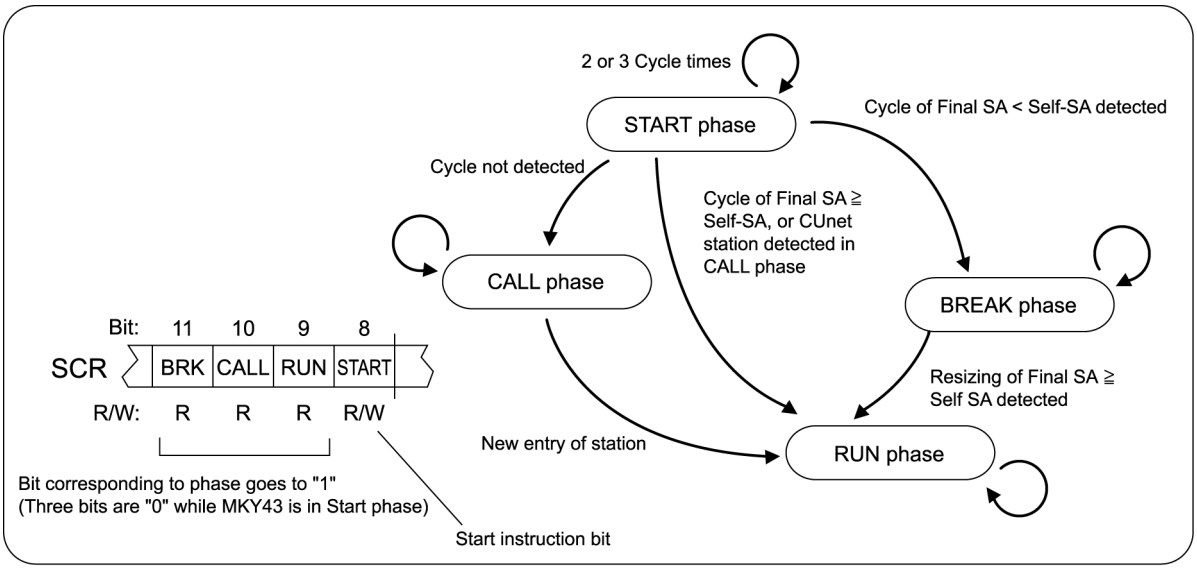

2 or 3 Cycle times
START phase
Cycle of Final SA < Self-SA detected
Cycle not detected
Cycle of Final SA ≧ Self-SA, or CUnet station detected in CALL phase
CALL phase
BREAK phase
Bit: 11 10 9 8
SCR BRK CALL RUN START
R/W: R R R R/W
Resizing of Final SA ≧ Self SA detected
New entry of station
RUN phase
Bit corresponding to phase goes to "1"
(Three bits are "0" while MKY43 is in Start phase)
Start instruction bit

Fig. 4.2 Phase Transition of MKY43 and Corresponding Bits of SCR

The "RUN phase" means the stage in which the CUnet operates normally. Bit 9 (RUN) of the SCR changes to "1". When the MKY43 is in the RUN phase, the user system program can use the following communications:

(1) When data transferred to other CUnet stations is written to the owned area of the self-station in Global Memory (GM), the data is copied to the same address in GM of other CUnet stations.
(2) The user system program can reference data copied from other CUnet stations by reading the owned area of other CUnet stations in GM.
(3) The user system program can mail the dataset to a specified CUnet station.
(4) The user system program can receive the dataset mailed to the self-station.

The "CALL phase" means the stage in which the CUnet is waiting to be connected. Bit 10 (CALL) of the SCR changes to "1". When all CUnet stations except the self-station connected to the network are not started, they enter this phase. The CALL phase is continued until packets can be transmitted and received to and from other CUnet stations.

The "BREAK phase" means the stage in which the self-station cannot enter a cycle. Bit 11 (BRK) of the SCR changes to "1". The BREAK phase is continued until other CUnet stations perform resizing to permit the self-station to enter a cycle.

Reference For details about resizing, refer to ***"4.4.2 Resizing of Cycle Time"***. A CUnet station with unstable hardware may cause the MKY43 to stop in the START phase to start the network. In this case, refer to ***"4.1.8.3 Stop Exception"*** to remove the instability.

4.1.5 Protection against Misoperation

The MKY43 has the following protective functions to prevent misoperation by the user system program (Fig. 4.3).

(1) "1" can be written to the GMM bit of the SCR only when the START bit of the SCR is "0".
(2) When the START bit of the SCR (System Control Register) is "1", any memory area other than the owned area in GM of the self-station is write protected.
(3) The BCR (Basic Control Register) can be written only when the START bit of the SCR is "0" and the GMM bit is "1".
(4) Dataset can be sent and received only when the RUN bit of the SCR is "1" (RUN phase).

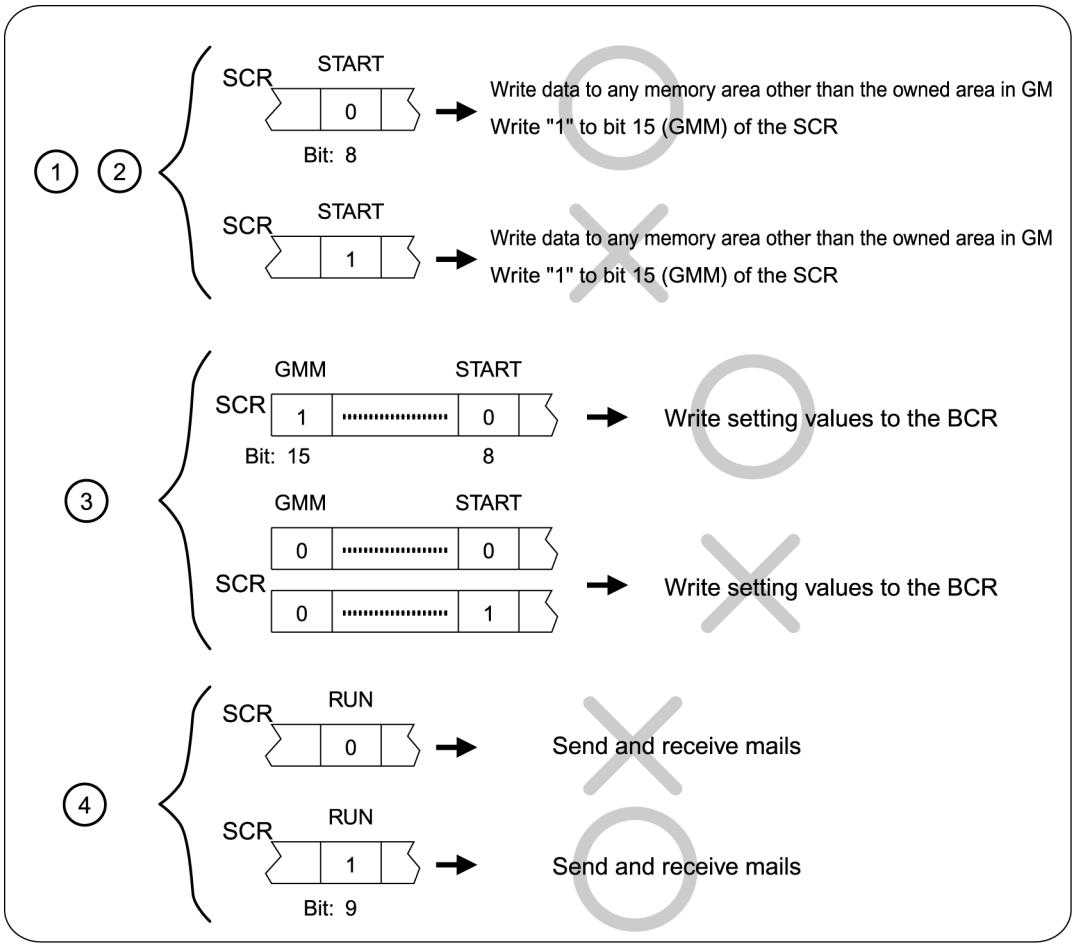


Fig. 4.3 Write Protection

Reference For details of the GMM bit of the SCR, refer to ***"4.4.8 Global Memory Monitor (GMM) Function"***.

4.1.6 Cycle Time of CUnet

The cycle time of a CUnet consisting of the MKY43 is determined by Equations 4.1 and 4.2 defined by the CUnet protocol. The CUnet cycle time is the response time for memory data sharing.

Equation 4.1 Frame Time = (LOF + FS + 1) × 2 × T_{BPS} [s]

Equation 4.2 Cycle Time = Frame Time × (FS + PFC + 1) [s]

For example, when FS = 03H, LOF = 151, PFC = 2, and baud rate = 12 Mbps (T_{BPS} = (1/12 × 10^6) ≈ 83.3 ns), the frame time and cycle time are calculated as follows:

Frame Time = (151 + 3 + 1) × 2 × (1/12 × 10^6) = 25.833 μs

Cycle Time = 25.833 μs × (3 + 2 + 1) = 155 μs

In a CUnet, LOF (Length Of Frame) is fixed at "151" and PFC (Public Frame Count) is fixed at "2". When using the frame option described in ***"4.4.9 Frame Option [for HUB]"***, the LOF is fixed at "256".
Final station (FS) values are stored in the FSR (Final Station Register) in registers of the MKY43. The initial FS value in a CUnet is "63 (3FH)". If resizing described in ***"4.4.2 Resizing of Cycle Time"*** is not performed, the value stored in the FSR is "63 (3FH)".

Reference The cycle time at each FS value calculated by Equations 4.1 and 4.2 is shown in ***"Appendix 1 Cycle Time Table"***.

4.1.7 Detailed Timing during Cycle

The user system can recognize the detailed timing during the cycle proceeding with frame transition in the MKY43.
To recognize the detailed timing during a cycle, the user system program needs to read the SCR.
Each value of bits 0 to 6 (ST0 to ST6) of the SCR indicates Station Time (ST) (Fig. 4.4).
When each value of bits 0 to 6 (ST0 to ST6) of the SCR corresponds to the setting values preset in a given register, the MKY43 can output interrupt triggers called "alarm". For details, refer to ***"4.5 Interrupt Trigger Generation Function"***.

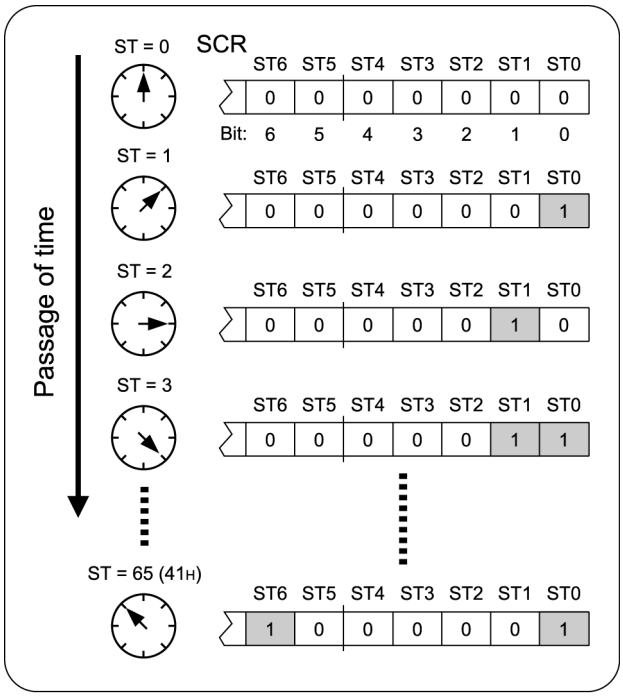


Fig. 4.4 Station Times Indicated by Bits 0 to 6 of SCR

4.1.8 Network Stop

The MKY43-mounted CUnet station stops its network when:

(1) "0" is intentionally written to the START bit of the SCR (System Control Register)
(2) SNF (Station Not Found): No link with CUnet stations other than the self-station could be established 32 cycle times consecutively
(3) OC (Out of Cycle): Resizing by other CUnet stations caused timing loss to send self-station packets at cyclic time sharing

By writing "0" to the START bit of the SCR, even if the MKY43 is in the START, CALL, RUN, or BREAK phase, the user system program running on the user CPU connected to the MKY43 can stop the network intentionally. At this network stop, the RUN, CALL, and BRK bits of the SCR also change to "0".

Network stop by SNF in (2) and OC in (3) occurs only when the MKY43 is in the RUN or BREAK phase even while the user system program running on the user CPU connected with the MKY43 is proceeding according to any algorithm.
At network stop by SNF, the RUN bit and START bit of the SCR change to "0" and SNF (bit 13) changes to "1".
At network stop by OC, the RUN bit and the START bit of the SCR change to "0" and OC (bit 12) changes to "1".

When the network is stopped, the MKY43 can output interrupt triggers. For details, refer to ***"4.5 Interrupt Trigger Generation Function"***.
When the user system program writes "1" to the START bit of the SCR or when a hardware reset is activated, the SNF bit and OC bit of the SCR are cleared to "0".

When network stop by OC occurs in the MKY43, the user system program must perform processing based on ***"Appendix 3 Processing when Network Stop by OC (Out of Cycle) occurs"***.

4.1.8.1 Details of SNF (Station Not Found)

Network stop by SNF occurs when the following events in the RUN phase cause the self-station to be isolated:

(1) Disconnection from network, network cable breaking, and damage to receiver parts
(2) Intentional stop of all CUnet stations other than the self-station

In these cases, all links with other CUnet stations are unestablished. The MKY43 regards the self-station as being isolated if a cycle in which no link with any CUnet station is established continues for 32 times. This causes network stop by SNF.
For the MKY43, network stop by SNF (Station Not Found) also occurs if a cycle in which no packet can be received from any CUnet station due to the cause in the above (1) or (2) continues for 32 times in the BREAK phase.

4.1.8.2 Details of OC (Out of Cycle)

Network stop by OC occurs when resizing by another CUnet station in the RUN phase prevents packet transmission of data in the owned area of the self-station. For example, if another CUnet station is resized to "1FH" when the SA of the self-station is "20H", the cycle is reduced and the self-station follows the FS, causing timing loss to send packet. If another CUnet station is resized to "20H" when the SA of the self-station is "20H" and OWN is "02H", the timing at packet sending of a part ("21H") of the owned area of the self-station is also lost. This causes network stop by OC. Network stop by OC occurs when the MKY43 detects resizing preventing packet sending of data in the owned area of the self-station.

4.1.8.3 Stop Exception

If a CUnet station has a continuously unstable power supply immediately after power-on, network stop by SNF (Station Not Found) may occur immediately after a start is made by the following sequence. The following is a stop sequence of a CUnet constructed by two CUnet stations.

(1) The user CPU writes "1" to the START bit of a CUnet station and this CUnet station enters the CALL phase.
(2) "1" is also written to the START bit of another CUnet station and this CUnet station and the above CUnet station enter the RUN phase.
(3) If stability after power-on of a CUnet station is delayed and a hardware reset is activated again, the START bit returns to "0".
(4) Another CUnet station stops by SNF after 32 cycles.
(5) The program starts again from the beginning, "1" is written to the START bit in a CUnet station and the CUnet station enters the CALL phase.
(6) Because the network is stopped by SNF, another CUnet station does not start again.

If the user system in this example "operates at 12 Mbps", the time required for the above sequences (1) to (6) to proceed is about 80 ms. Such cases occur in a system with a continuously unstable power supply after power-on. If the user system program waits just until it enters the RUN phase, it cannot get to the next step. The CUnet station with the MKY43 should be configured to cancel a hardware reset after the power supply stabilizes immediately after power-on.

The user system program should use such an algorithm to detect network stop by SNF or by OC and perform suitable processing for the user system (such as writing "1" to the START bit to restart the network).

4.2 Use of GM

This section describes the use of Global Memory (GM) where data is shared in the CUnet.

4.2.1 Details of Owned Area

GM in the MKY43 is 512-byte memory where “sixty-four” 8-byte Memory Blocks (MBs) defined in the CUnet protocol are arranged consecutively. Each MB is an area at each corresponding SA that is owned by the CUnet station (Fig. 4.5).

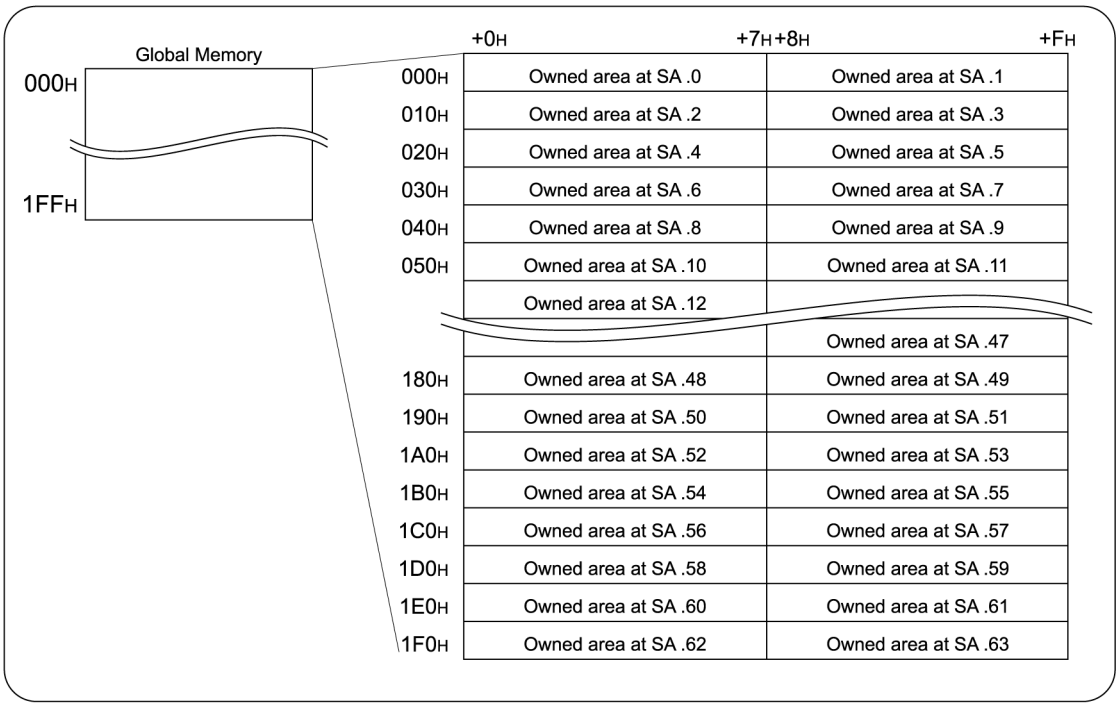

Global Memory
000H
1FFH
+0H
+7H
+8H
+FH
000H Owned area at SA .0 Owned area at SA .1
010H Owned area at SA .2 Owned area at SA .3
020H Owned area at SA .4 Owned area at SA .5
030H Owned area at SA .6 Owned area at SA .7
040H Owned area at SA .8 Owned area at SA .9
050H Owned area at SA .10 Owned area at SA .11
Owned area at SA .12
Owned area at SA .47
180H Owned area at SA .48 Owned area at SA .49
190H Owned area at SA .50 Owned area at SA .51
1A0H Owned area at SA .52 Owned area at SA .53
1B0H Owned area at SA .54 Owned area at SA .55
1C0H Owned area at SA .56 Owned area at SA .57
1D0H Owned area at SA .58 Owned area at SA .59
1E0H Owned area at SA .60 Owned area at SA .61
1F0H Owned area at SA .62 Owned area at SA .63

Fig. 4.5 Global Memory (GM)

The MKY43 can expand an owned area by the setting of OWN widths defined in “Increased Practicality” in the CUnet protocol.

The owned area depends on the SA and OWN width stored in the BCR (Basic Control Register). The MB with an OWN width corresponding to an SA is an owned area (Fig. 4.6). For example, with SA = 6 and OWN = 2, the MKY43 owns a 16-byte area between MB 6 and 7 (GM: 030H and 03 FH).

The owned area in the CUnet is area to send (copy) data to other CUnet stations. In the MKY43, the owned area can be always written, but GM other than the owned area is write protected when the START bit of the SCR is “1”.

When using GM in a CUnet, a write-enable area and a read-only area are definitely separated and simultaneous write and overwrite to the same address does not occur.

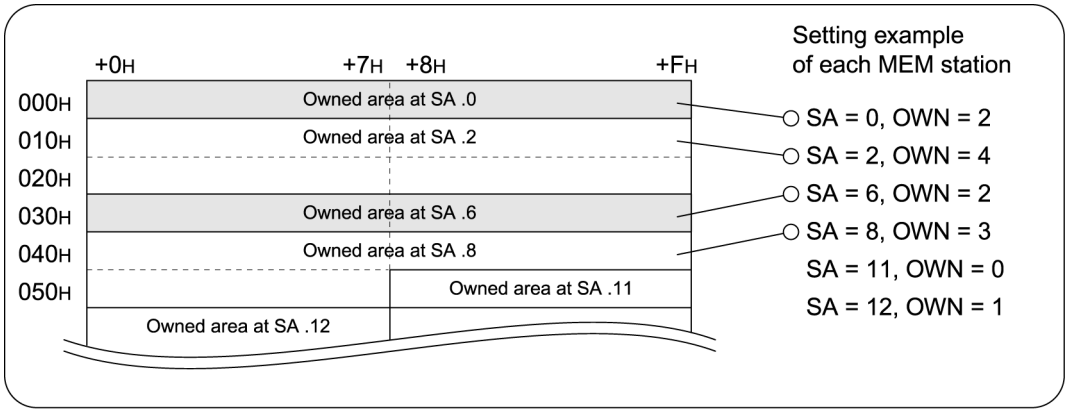


Fig. 4.6 Expansion of Owned Area

An owned area must not be duplicated in any CUnet stations constituting a CUnet. For example, if SA is set to 3 and OWN to 2 for one MKY43, SA must not be set to 4 for another MKY43. An owned area must not be duplicated when performing the setting described in sections ***"3.6 Setting Station Addresses and Owned Area"***, and item (2) of section ***"4.1.3 Initialization and Start-up of Communication"***.
Unless duplicated, an owned area can be set widely. For example, in a CUnet consisting of two MEM stations, each MEM station can have a "256-byte" owned area.

When the OWN width value of the BCR is "00H", the OWN width is treated as "1". If the value to which the SA value and OWN value stored in the BCR are added exceeds "64 (40H)", the value exceeding "64" is ignored. For example, if the SA value is "62 (3EH)" and the OWN value is "03H", the OWN width is "2". If the SA value is "32 (20H)" and the OWN value is "63 (3FH)", the OWN width is "32".

4.2.2 Data Hazards

When another CUnet station reads datasets during the writing of the datasets such as character strings across addresses, character strings with written data and old data mixed may be read. This phenomenon is called "data hazards". Data hazards do not occur when handling data within the width of the bus connecting the user CPU and MKY43.

When handling data that is wider than the width of the bus connecting the user CPU and MKY43, the following data hazards occur (Fig. 4.7).

(1) When the user CPU connected to the MKY43 via the 8-bit width data bus reads 16-bit width data from the area in GM owned by the CUnet station, access must be made "twice".
(2) When data changes with data copying from another CUnet station based on the sharing of memory data between the user system program's first and second accesses to GM, timing problems disable reading of correct data (5634H read in Fig. 4.7).
(3) In this case, the read data is erroneous data where data hazards occurred.

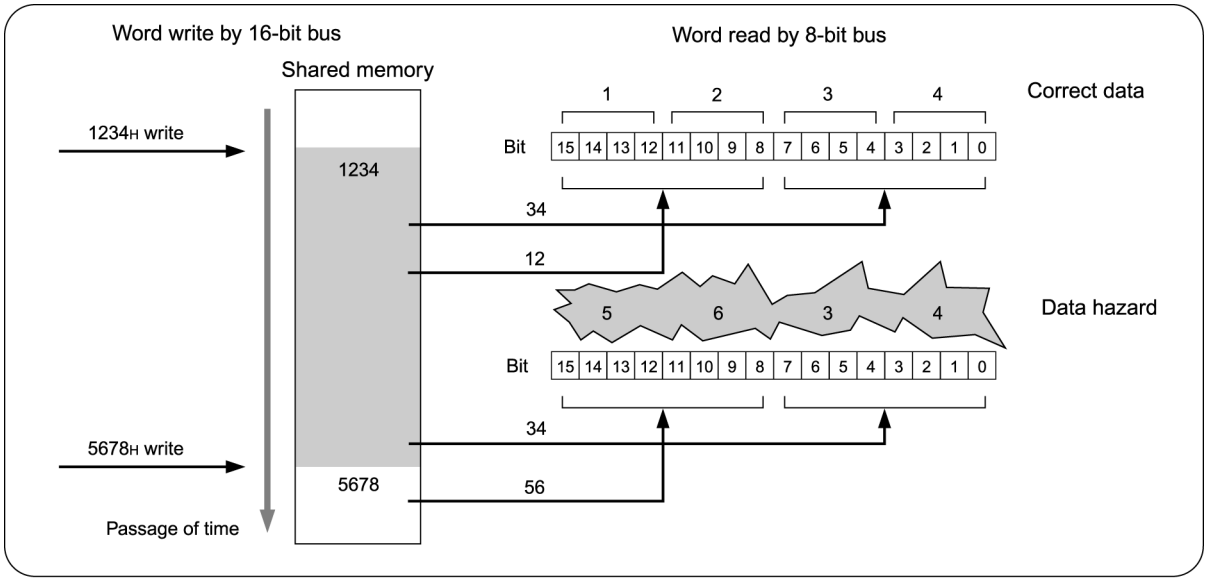


Fig. 4.7 Mechanism of Data Hazard

Data hazards also occur during writing (Fig. 4.8).

For example, when the user CPU connected to the MKY43 via the 8-bit width data bus writes "1234H", writing must be performed "twice".

When the old data "ABCDH" is copied to another CUnet station based on the sharing of memory data during the separate writing of "34H" and "12H" data, another CUnet station that reads this data will recognize it as "AB34H" (nonexistent data causing data hazards) instead of "1234H" or "ABCDH".

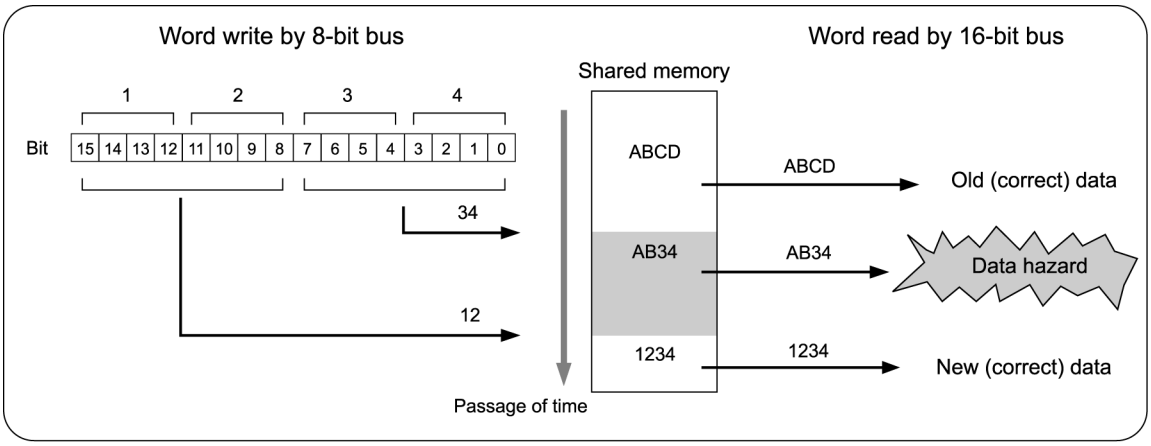


Fig. 4.8 Data Hazards during Writing

The MKY43 has the "hazard protection function" as the function to prevent the data hazard occurring when handling data wider than the bus width.

4.2.2.1 Hazard Protection Function

In Global Memory (GM) in the MKY43, sixty-four 8-byte Memory Blocks (MBs) are arranged. If one MB as a unit can be read or written collectively, the data by MB can be protected against the data hazard. The MKY43 has the Hazard Protection Buffer to perform this protection.

4.2.2.2 How to Use Read Hazard Protection

The MKY43 has two buffers, the RHPB0 (Read Hazard Protection Buffer 0) and the RHPB1 (Read Hazard Protection Buffer 1), to read data of one MB from GM collectively.

The RHPB0 is controlled by the RHCR0 (Read Hazard Control Register 0). The RHPB0 and the RHCR0 are present respectively in a register area with a different address to that of GM. Use the RHPB0 and the RHCR0 by the following procedure (Fig. 4.9):

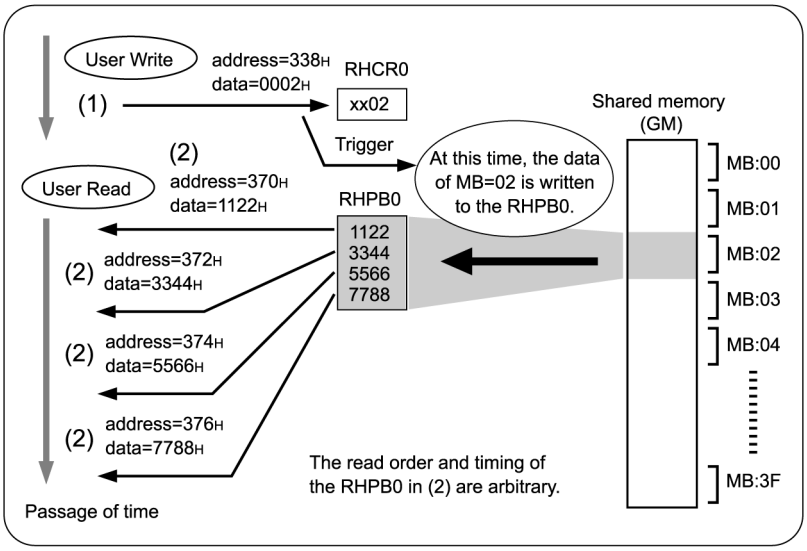


Fig. 4.9 Reading by Using Hazard Protection Function

(1) Write the MB value to be read, to the RHCR0. Thanks to the write, the data of the specified MB is read from the GM collectively and is stored to the RHPB0.
(2) The user can read the data from the RHPB0 at any time.
(3) When reading another MB, repeat the steps (1) and (2) above.

Similarly, the RHPB1 (Read Hazard Protection Buffer 1) is controlled by the RHCR1 (Read Hazard Control Register 1).

Since each of the RHPB0 and RHPB1 is an independent function, they will not interfere with each other. So, it is useful to use the RHPB0 and RHPB1 for different programs separately; for example, the RHPB0 is used by the user main program, and the RHPB1 is used by the user interrupt handling program.

4.2.2.3 How to Use Write Hazard Protection

The MKY43 has two buffers, the WHPB0 (Write Hazard Protection Buffer 0) and the WHPB (Write Hazard Protection Buffer 1), to write 8-byte (64-bit) data collectively to one Memory Block (MB) in GM.

The WHPB0 is controlled by the WHCR0 (Write Hazard Control Register 0). The WHPB0 and the WHCR0 are present respectively in a register area with a different address to that of GM.
Use the WHPB0 and the WHCR0 by the following procedure (Fig. 4.10):

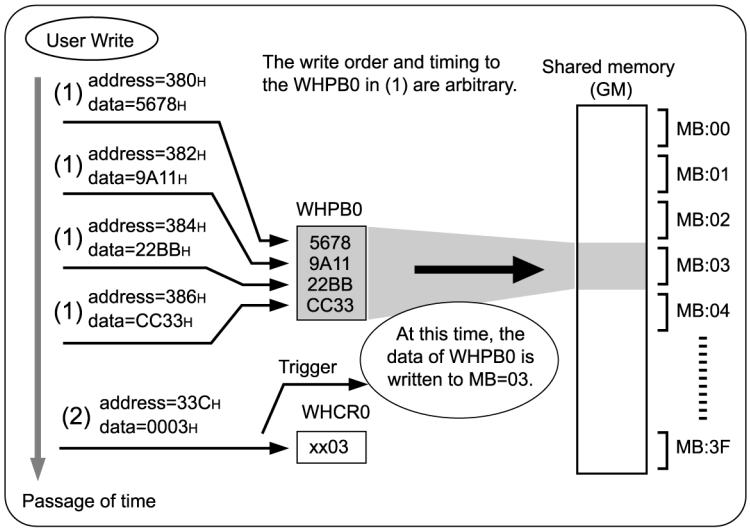


Fig. 4.10 Writing by Using Hazard Protection Function

(1) The user writes all data (8 bytes, that is, 64 bits) for one MB to the WHPB0 at any time.
(2) Write the MB value to be written, to the WHCR0. Thanks to the write, all data of the WHPB0 is written to the specified MB collectively.
(3) When writing data to another MB, repeat the steps (1) and (2) above.

In the following cases, the Global Memory (GM) is write-protected. So, the WHCR0 is also write-protected.

- When the GMM bit of the System Control Register (SCR) is "1"
- When the START bit of the SCR is "1" and any MB value other than that in the owned area is written to the WHCR0

Similarly, the WHPB1 (Write Hazard Protection Buffer 1) is controlled by the WHCR1 (Write Hazard Control Register 1).

Since each of the WHPB0 and WHPB1 is an independent function, they will not interfere with each other. So, it is useful to use the WHPB0 and WHPB1 for different programs separately; for example, the WHPB0 is used by the user main program, and the WHPB1 is used by the user interrupt handling program.

Caution If all of the 8-byte (64-bit) data has not been written to the WHPB0 during the operation of the step (1) above, the previous data remains in the byte area where the write had not been performed. In this state, if the operation of the step (2) above is performed, a mixed data of the newly written data and the previous data remaining in the buffer is written to the specified MB.

4.2.2.4 Protection Against Data Hazard without Hazard Protection Function

Data hazards are caused by data changes (due to data copying based on the sharing of memory data) during several accesses from the user CPU. Data hazards can be avoided without using the hazard protection function if the user CPU can make several accesses at the timing when data copying based on the sharing of memory data does not occur.

In the CUnet, the timing when data copying based on the sharing of memory data occurs can be recognized by Station Time (ST). The user system program can recognize ST by reading bits 0 to 6 (ST0 to ST6) of the System Control Register (SCR) of the MKY43 (refer to ***"4.1.7 Detailed Timing during Cycle"***).
Specific examples are shown below:

(1) When making several read accesses to the memory block corresponding to SA "03H" (addresses "018H to 01FH" of the GM), the user system program continues to read the SCR until the ST goes to other something than "03H" and waits for read access to memory.
(2) If ST is not "03H" after reading the SCR (data hazards may not occur), the user system program immediately makes several read accesses.

The above methods are applicable only when the user CPU is fast enough for the CUnet cycle and access after recognizing timing by the ST is terminated by the arrival of the timing of waiting until the next data hazard may occur. For example, the program proceeds to interrupt handling during above steps (1) and (2), making it unclear when read accesses are terminated. Such user programs should be avoided.

Timing-sensitive user system programming generally tends to be more difficult. Therefore, the hazard protection function should be used to avoid data hazards.
Reading the SCR to recognize the operation timing of the CUnet is also useful for purposes other than avoiding data hazards in the user system program.

The scope (target address range) of avoidable data hazard by the hazard protection function is one memory block (8 bytes). When handling data exceeding this value (such as 128-bit data or character strings of 9 or more bytes), create the user system program based on the description in this section.

4.2.3 Quality Assurance of GM Data

The MKY43 with CUnet protocol assures CUnet station-to-CUnet station (N-to-N) communications on a network.

As defined in the CUnet protocol, this assured status is indicated in registers by the receiving status and link status. The MKY43 has a function enabling the user system program to monitor each status easily.

This section describes registers and status monitoring functions related to data quality assurance of Global Memory (GM) data.

For the definitions of the receiving status and link status, refer to ***"Data Quality Assurance"*** in ***"CUnet Introduction Guide"***.

4.2.3.1 Status Indication by Registers

In the MKY43, the receiving status and link status defined in the CUnet protocol are indicated by the Receive Flag Register (RFR) and Link Flag Register (LFR). The RFR and LFR are 64-bit registers (Fig. 4.11).

Since a CUnet can be constructed using up to 64 CUnet stations, bit 0 in each register corresponds to the Station Address (SA) = 0 and Memory Block (MB) = 0, bit 1 to SA = 1 and MB = 1, and bit 63 to SA = 63 and MB = 63.

The user system program reads the RFR and LFR to recognize bits set to "1", and thereby determining the assured status of shared memory data in GM.

(1) When recognizing whether data in MBs other than the owned area is the latest data copied from other CUnet stations, read the RFR containing individual flag bit values guaranteeing that data in individual MBs is fetched by the latest cycle.

(2) When recognizing whether there is any CUnet station incapable of copying data in the owned areas, read the LFR containing individual flag bit values guaranteeing that data in individual MBs is fetched by the latest cycle and that data in the MB of the self-station is copied correctly to individual CUnet stations.

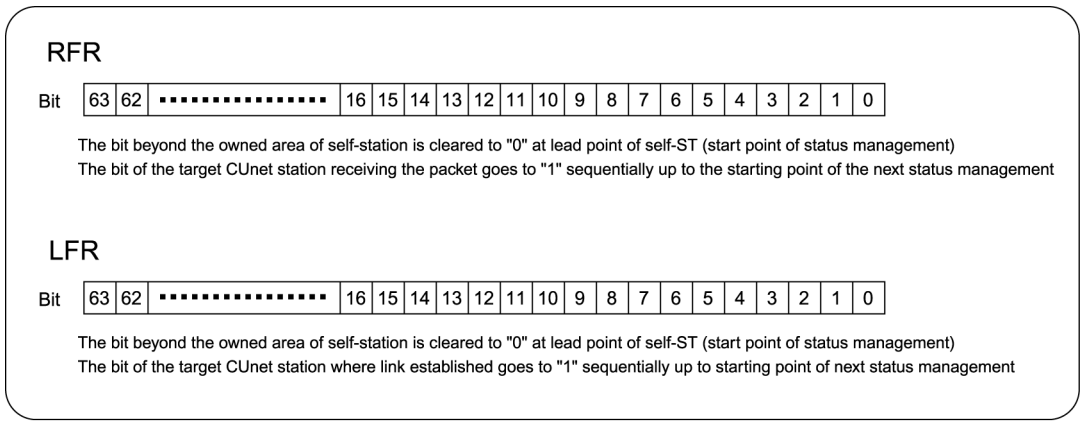

RFR
Bit
63 62 ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
The bit beyond the owned area of self-station is cleared to "0" at lead point of self-ST (start point of status management)
The bit of the target CUnet station receiving the packet goes to "1" sequentially up to the starting point of the next status management
LFR
Bit
63 62 ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
The bit beyond the owned area of self-station is cleared to "0" at lead point of self-ST (start point of status management)
The bit of the target CUnet station where link established goes to "1" sequentially up to starting point of next status management

Fig. 4.11 64-bit RFR and LFR

4.2.3.2 Starting Point of Status Management and Exception

In the MKY43, the real-time status based on cycle transition at cyclic time sharing is reflected in the status of RFR and LFR. The lead point of ST corresponding to the SA of the self-station is the starting point of status management (Fig. 4.12).

The status of the RFR and LFR is managed every cycle. Except for the case described in section ***"4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation"***, RFR and LFR are cleared to "0" at the starting point of status management. The bits of RFR and LFR corresponding to the owned areas of the self-station are fixed to "1" while the START flag of the SCR (System Control Register) is set to "1".

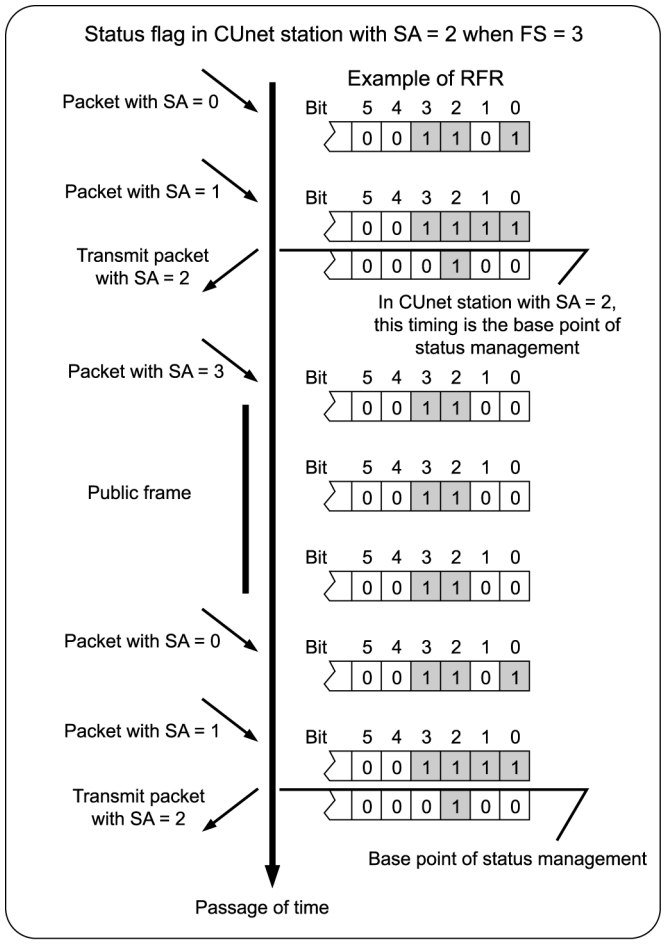

Status flag in CUnet station with SA = 2 when FS = 3
Example of RFR
Packet with SA = 0
Packet with SA = 1
Transmit packet with SA = 2
Packet with SA = 3
Public frame
Packet with SA = 0
Packet with SA = 1
Transmit packet with SA = 2
Bit 5 4 3 2 1 0
0 0 1 1 0 1
0 0 1 1 1 1
0 0 0 1 0 0
In CUnet station with SA = 2, this timing is the base point of status management
0 0 1 1 0 0
0 0 1 1 0 0
0 0 1 1 0 0
0 0 1 1 0 1
0 0 1 1 1 1
0 0 0 1 0 0
Base point of status management
Passage of time

Fig. 4.12 Starting Point of Status Management

The MKY43 has a monitoring function described in section ***"4.4.8 Global Memory Monitor (GMM) Function"*** in addition to functions defined in the CUnet protocol. The SA of the self-station is undefined in the MKY43 that operates as a GMM station by this function. This means that there is no "starting point of status management" in the GMM station. Therefore, in the GMM station, the "starting point of status management" is used as the lead point (Station Time = 0) of a cycle. At the lead point of a cycle, all bits of the RFR are cleared to "0" and the bits for which receiving is established change to "1" sequentially. Since the GMM station is not linked with another CUnet station, the status of the LFR bits has no meaning, resulting in invalid data.

Caution When (except as described in section ***"4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation"***) the RFR and LFR are read immediately after the starting point of status management, "0" is read from bits other than the owned areas of the self-station. After understanding the cyclic time sharing, read the RFR and LFR at the appropriate time.

4.2.3.3 Link Group Register (LGR)

The status of the Link Flag Register (LFR) changes dynamically according to the constantly repeated cycles. This change is very fast. For example, if the baud rate is 12 Mbps and the Final Station (FS) value is "01H", the frame time is 25.5 μs. Thus, the status changes every 25.5 μs and is updated every 102 μs of one cycle time.

If the user system manages the status of the LFR in detail, the status changes so fast that the program cannot run sufficiently. To solve this problem, the MKY43 has a group setting function that helps monitor the LFR status.

The MKY43 has the 64-bit Link Group Register (LGR). The LGR monitors the status of the LFR. Each LGR bit corresponds to each LFR bit. The user system program can write "1" or "0" arbitrarily to the LGR bits.

The MKY43 clears the LFR to "0" at the starting point of status management and then sequentially detects the LFR bits corresponding to the LGR bits at "1". If all the bits to be detected go to "1", the MKY43 considers "Link OK". If any of the bits to be detected is "0" immediately before the starting point of the next status management after the cycle proceeded, the MKY43 considers "Link NG (No Good)" (Fig. 4.13).

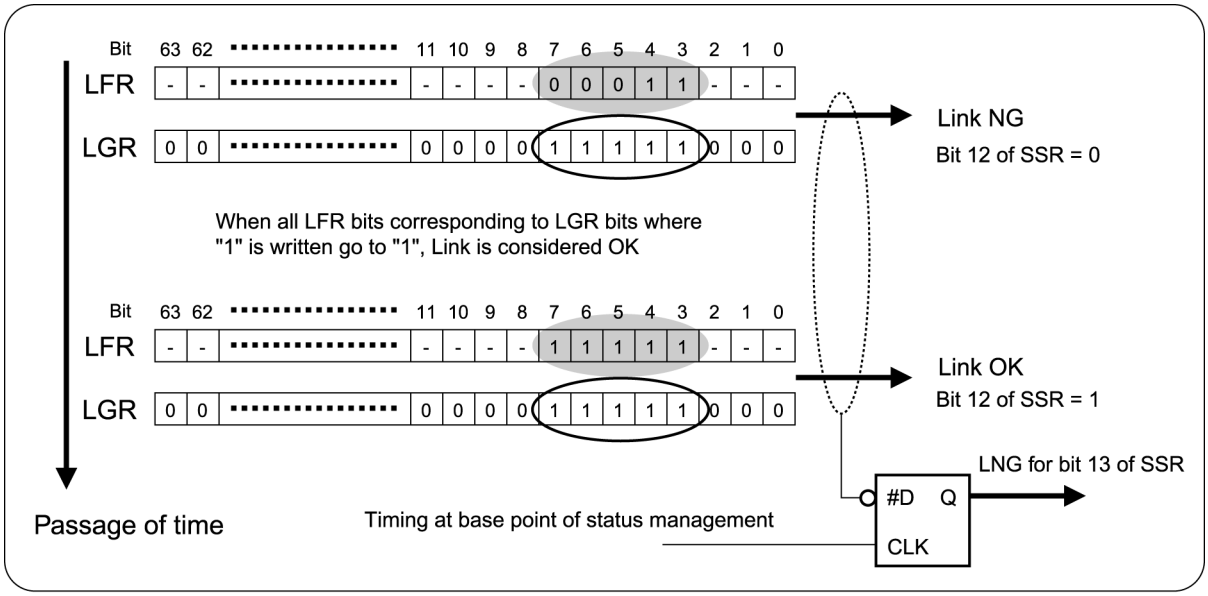

Bit 63 62 ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ 11 10 9 8 7 6 5 4 3 2 1 0
LFR - - ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ - - - - 0 0 0 1 1 - - -
LGR 0 0 ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ 0 0 0 0 1 1 1 1 1 0 0 0
Link NG
Bit 12 of SSR = 0
When all LFR bits corresponding to LGR bits where "1" is written go to "1", Link is considered OK
Bit 63 62 ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ 11 10 9 8 7 6 5 4 3 2 1 0
LFR - - ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ - - - - 1 1 1 1 1 - - -
LGR 0 0 ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ 0 0 0 0 1 1 1 1 1 0 0 0
Link OK
Bit 12 of SSR = 1
LNG for bit 13 of SSR
#D Q
CLK
Passage of time
Timing at base point of status management

Fig. 4.13 LFR Monitoring by LGR

This result is notified to the user system by the following two methods:

(1) The result is indicated by the flag bit where "1" is true in bit 13 (LNG: Link group No Good) and bit 12 (LOK: Link group OK) of the SSR.

Except for the special case described in ***"4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation"***, the LOK flag bit is cleared to "0" at the starting point of status management.

The LNG flag bit samples the result in the immediately preceding cycle at the starting point of status management and holds the sampled result for the next one cycle (Fig. 4.13).

(2) The MKY43 can output interrupt triggers.
The user system program can recognize "Link OK" or "Link NG" by receiving interrupt trigger. For details, refer to ***"4.5 Interrupt Trigger Generation Function"***.

As described above, the user system program can monitor the LFR status collectively by pre-setting the bits to the LGR bits for monitoring the LFR status.

Caution If the user system program monitors the link by method (1) above, read the SSR at the appropriate time after understanding cyclic time sharing.

4.2.3.4 Member

The CUnet operation in a stable environment does not allow the occurrence of "Dead Link" defined in the CUnet protocol and LNG (Link Group No Good) during status management (LGR bits at "1") described in ***"4.2.3.3 Link Group Register (LGR)"***.
"Dead Link" and LNG occur when the "CUnet station disconnects" or "trouble with receiving or sending packet occurs due to environmental problems including external noise". Instantaneous "Dead Link" is recovered by the next cycle based on cyclic time sharing that is a CUnet operating principle.

General communications conventionally use an error handling algorithm when recovery fails after "three" retries (resending) when "trouble with receiving or sending packet occurs due to environmental problems including external noise".

The MKY43 has two registers to help manage accordingly: 64-bit Member Flag Register (MFR) and Member Group Register (MGR). In the MKY43, the concept of using this management form is called a "member" (Fig. 4.14).

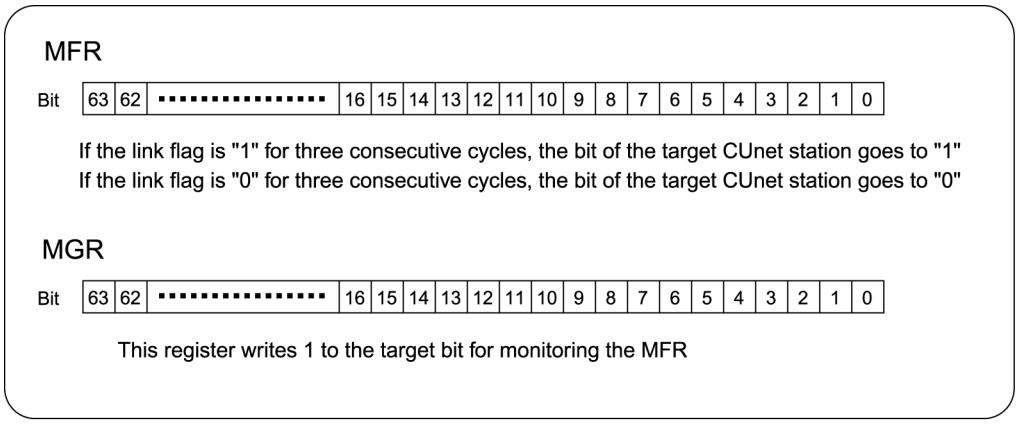

MFR
Bit
63 62 ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
If the link flag is "1" for three consecutive cycles, the bit of the target CUnet station goes to "1"
If the link flag is "0" for three consecutive cycles, the bit of the target CUnet station goes to "0"
MGR
Bit
63 62 ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
This register writes 1 to the target bit for monitoring the MFR

Fig. 4.14 64-bit MFR and MGR

4.2.3.5 Member Flag Register (MFR)

In the Member Flag Register (MFR), like the Link Flag Register (LFR), bit 0 corresponds to the CUnet station with the Station Address (SA) = 0, bit 1 to the CUnet station with SA = 1, and bit 63 to the CUnet station with SA = 63 (3FH).
In the MFR flag bit, like the LFR flag, the lead point of the Station Time (ST) matching the Station Address (SA) is the starting point of status management.
When the MFR flag bit recognizes "Link established" consecutively three times at the starting point of status management, it changes to "1". Conversely, when the MFR flag bit recognizes Link unestablished consecutively three times at the starting point of status management in the CUnet station where the MFR is "1", it changes to "0". This method provides the MFR with a management function similar to general communications management.

When the user system "accepts instantaneous Dead Link as long as it is recovered by the cycle based on cyclic time sharing", the user system can recognize the assured state including global memory data recovery by reading the MFR. The MFR register is also effective for management of "disconnection of CUnet station". If a CUnet station disconnects, the MFR bit corresponding to the CUnet station changes from "1" to "0".

4.2.3.6 Member Group Register (MGR)

The MFR status is updated at the starting point of status management according to the consecutively repeated cycle. The MKY43 has a function (64-bit MGR) to reduce the burden on user system program detailed management of the MFR status.
The MGR monitors the MFR status. Each MGR bit corresponds to each MFR bit. The user system program can arbitrarily write "1" or "0" to the MGR bits. The MKY43 collectively detects the MFR bits corresponding to the MGR bits at "1" every one cycle immediately before the starting point of status management and makes a decision based on the following two items (Fig. 4.15):

1. The MGR does not match the MFR (MGR ≠ MFR).
2. The MFR bits corresponding to the MGR bits at "1" are at "0" (MGR > MFR).

This result is notified to the user system by the following two methods:

(1) Indicating the result where "1" is true in bit 4 (MGNE: Member group Not Equal) and bit 5 (MGNC: Member group Not Collect) of System Status Register (SSR)
The MGNE and MGNC flag bits are updated at the starting point of status management.

(2) The MKY43 can output interrupt triggers
The MKY43, if a given interrupt has been set for it, outputs interrupt triggers when bit 4 (MGNE) or bit 5 (MGNC) of SSR, mentioned in above (1), newly changes from "0" to "1". For this interrupt setting, refer to ***"4.5 Interrupt Trigger Generation Function"***.

In the MKY43, functions mentioned in above (1) and (2) do not function when all of the MGR bits are "0".

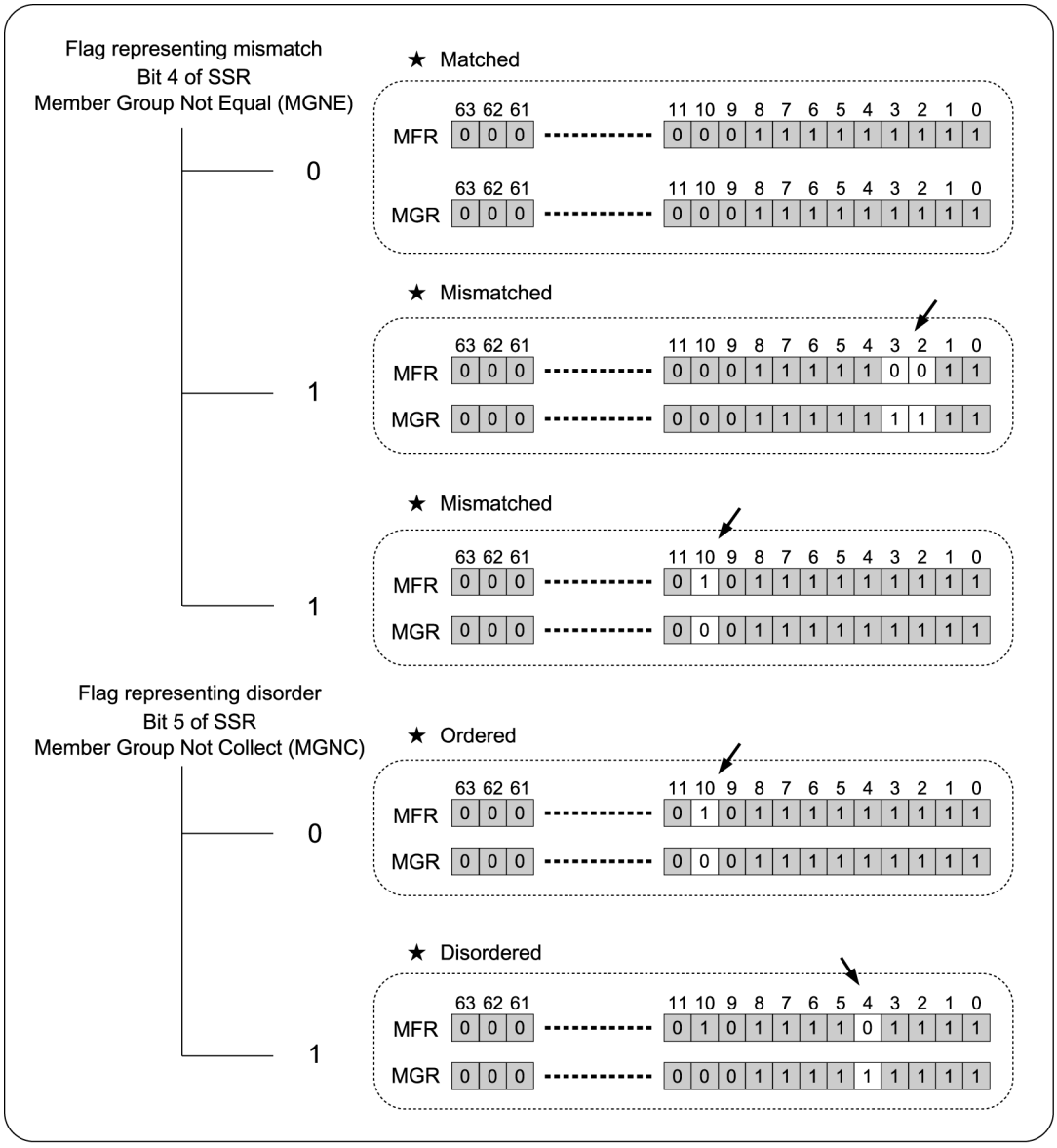


Fig. 4.15 MFR Monitoring by MGR and Bit Status of SSR

As described above, when the user system program presets the MGR bits for monitoring the MFR status, the user system can monitor the MFR status collectively.

For example, when monitoring the lack of a CUnet station, periodically read the SSR (System Status System) at the appropriate time while the user system program is running.
If bit 4 (MGNE: Member Group Not Equal) of the SSR is "0", the CUnet station corresponding to the bit where "1" was written beforehand to the MGR is not separated from the member. Stations other than the CUnet station corresponding to the bit where "1" was written beforehand to the MGR do not exist as a member. When permitting their existence, ensure that bit 5 (MGNC: Member Group Not Collect) of the SSR is "0".
When monitoring the above status by the "accepting interrupt triggers" method, the user system program does not need to periodically read the SSR.

4.2.3.7 Detection of Member Increase and Decrease

The MKY43 has a function (bit 14 (NM: New Member) and bit 15 (MC: Member Care) of the SSR (System Status Register)) to detect the bit transition of the MFR (Member Flag Register), regardless of the bit status of the MGR (Member Group Register).

New Member (NM) indicates the result (where "1" is true) with a flag bit when MFR bits change from "0" to "1" (member increase). Also, Member Care (MC) indicates the result (where "1" is true) with a flag bit when MFR bits change from "1" to "0" (member decrease).

The NM and MC bits of the SSR are updated at the starting point of status management. This result enables the output of interrupt triggers. For details, refer to ***"4.5 Interrupt Trigger Generation Function"***.

Managing the NM and MC bits enables the user system program to manage the member without using the MGR as described in ***"4.2.3.6 Member Group Register (MGR)"***.

4.2.4 Detection of Global Memory Data Transition

The MKY43 has a function to detect the data transition of global memory occurring when data in other CUnet stations are updated. This function enables construction of a user system algorithm so that global memory is read only when data transition is detected. This section describes the function to detect the data transition of global memory and its use.

4.2.4.1 Data Renewal Check Register (DRCR) for Setting Detection of Data Transition

The Data Renewal Check Register (DRCR) is used to detect data transition of global memory. Each bit of the 64-bit DRCR corresponds to each memory block constituting global memory; for example, bit 0 of the DRCR corresponds to memory block 0, bit 7 to memory block 7, and bit 63 to memory block 63 (3FH).
Writing "1" to the DRCR bits beforehand provides the following detection results when data transition occurs in the corresponding memory blocks.

(1) Bit 11 (DR: Data Renewal flag bit) of the SSR changes to "1". The user system program can recognize the data transition of global memory by monitoring the DR flag bit.
(2) Interrupt triggers can be output.
The user system program can recognize the data transition of global memory by accepting interrupt triggers. For details, refer to ***"4.5 Interrupt Trigger Generation Function"***.

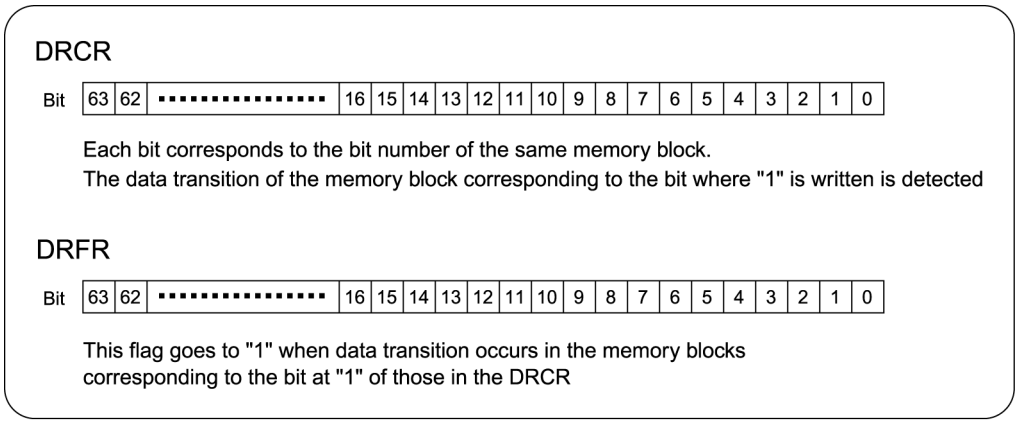

DRCR
Bit
63 62 ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Each bit corresponds to the bit number of the same memory block.
The data transition of the memory block corresponding to the bit where "1" is written is detected
DRFR
Bit
63 62 ▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪▪ 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
This flag goes to "1" when data transition occurs in the memory blocks
corresponding to the bit at "1" of those in the DRCR

Fig. 4.16 64-bit DRCR and DRFR

Writing "1" to multiple bits of the DRCR beforehand also provides the detection results when data in one or more memory blocks change. In this case, the MKY43 also has a flag bit (the 64-bit DRFR: Data Renewal Flag Register) indicating in which memory block the data transition occurred. The bit arrangement of the DRFR corresponds to each memory block (Fig. 4.16). Of the DRFR bits, the bit corresponding to the memory block where data changed is set to "1". The user system program can recognize the memory block where data changed by recognizing the DRFR flag bit.

Caution Bit 11 (DR) of the SSR and DRFR function only when "1" is set to the DRCR. The function to detect data transition does not operate for the memory block owned by the self-station (even if "1" is set to the target DRCR).

4.2.4.2 Transition Timing of DR Flag Bit and DRFR Bits from “0” to “1”

Bit 11 (DR: Data Renewal) of the SSR and each bit of the DRFR transits from “0” to “1” when packets are received from other CUnet stations and data in the global memory is updated for data copying based on sharing of received memory data (Fig. 4.17).

4.2.4.3 Transition Timing of DR Flag Bit and DRFR Bits from “1” to “0”

The timing of bit 11 (DR) of the SSR and each bit of the DRFR changing from “1” to “0” depends on the MKY43 usage environment as follows (Fig. 4.17):

(1) Bit 11 (DR) of the SSR and DRFR bits change from “1” to “0” at the lead point period of the time written to bits 8 to 14 of the IT0CR (if the DR bit of the INT1CR is “1”, at the lead point period of the time written to bits 8 to 14 of the IT1CR). Refer to the generation timing of data renewal interrupt described in ***“4.5.5 Precautions for Specifying Timing of Interrupt Trigger Generation”*** and ***“4.5.6 Precautions for Use of Data Renewal (DR) Interrupt Triggers”***.

(2) However, if the data renewal interrupt triggers described in ***“4.5 Interrupt Trigger Generation Function”*** is activated, bit 11 (DR) of the SSR and the DRFR bits freeze (remain unchanged) without changing to “0”. When the generation of data renewal interrupt triggers is cancelled by the user register operation, the status is reflected in the DRFR. For details, refer to ***“4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation”***.

(3) When bit 15 of the SCR (System Control Register) described in ***“4.4.8 Global Memory Monitor (GMM) Function”*** is “1”, bit 11 (DR) of the SSR and DRFR bits change from “1” to “0” at the lead point of the cycle (cycle time = 0). This occurs due to the non-existence of the self-station time of the MKY43 used as the GMM.

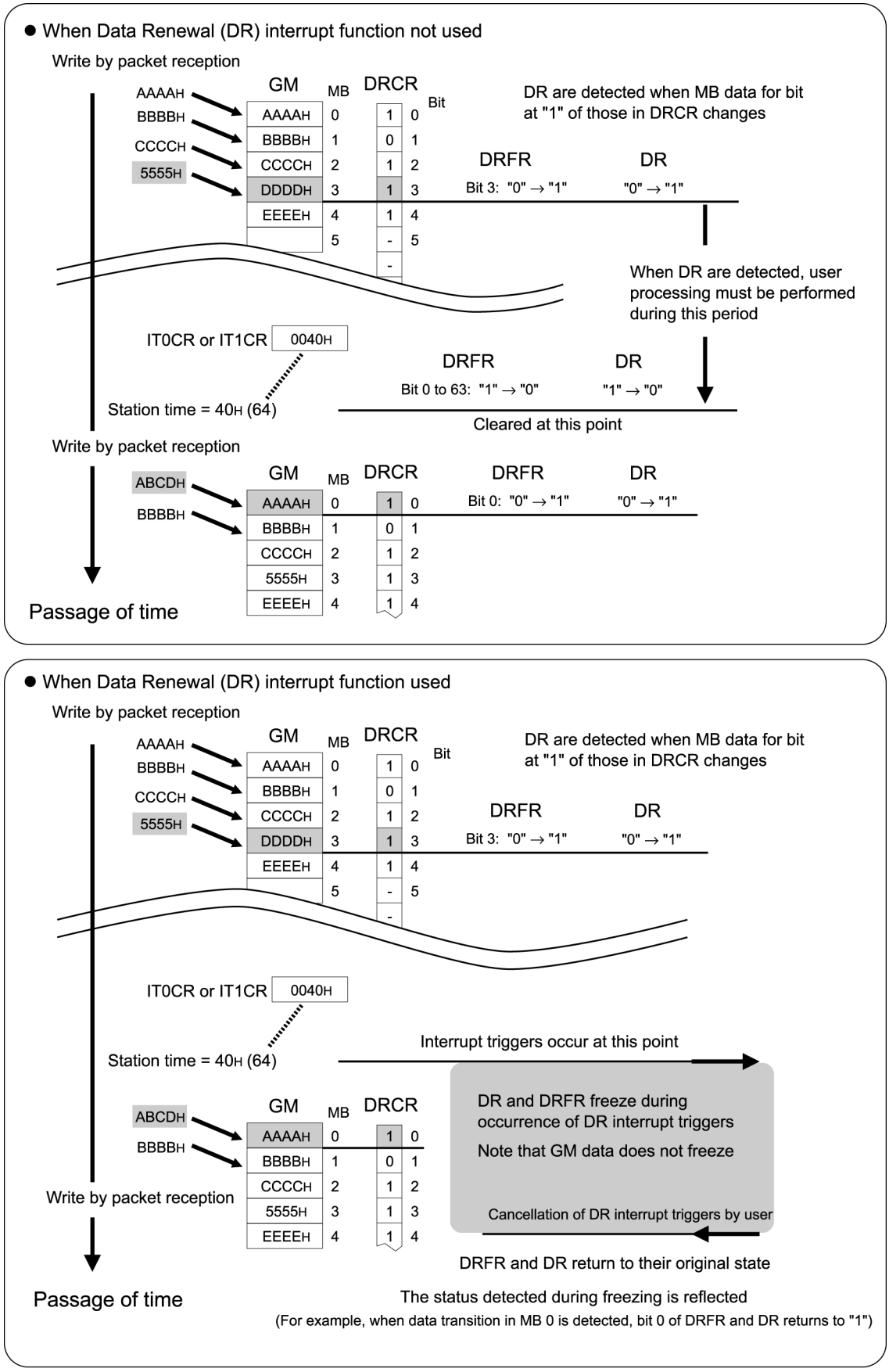

● When Data Renewal (DR) interrupt function not used
Write by packet reception
AAAAH
BBBBH
CCCCH
5555H
GM
MB
DRCR
Bit
DR are detected when MB data for bit at "1" of those in DRCR changes
DRFR
DR
Bit 3: "0" → "1"
"0" → "1"
When DR are detected, user processing must be performed during this period
IT0CR or IT1CR
0040H
Station time = 40H (64)
Bit 0 to 63: "1" → "0"
"1" → "0"
Cleared at this point
Write by packet reception
ABCDH
BBBBH
Bit 0: "0" → "1"
"0" → "1"
Passage of time
● When Data Renewal (DR) interrupt function used
Write by packet reception
Interrupt triggers occur at this point
DR and DRFR freeze during occurrence of DR interrupt triggers
Note that GM data does not freeze
Cancellation of DR interrupt triggers by user
DRFR and DR return to their original state
Write by packet reception
Passage of time
The status detected during freezing is reflected
(For example, when data transition in MB 0 is detected, bit 0 of DRFR and DR returns to "1")

Fig. 4.17 Outline of Data Renewal Detection for Time Passage

4.2.4.4 Precautions for Use of Detection of Data Transition

One cycle time in CUnet is very short. Perform user processing immediately after data renewal is detected. If user processing is not performed before the target memory block receives packets in the next cycle, the next data transition may not be detected or the user system may not respond even if the data transition is detected.

When using the data renewal (DR) interrupt trigger generating function, perform user system processing to avoid the above problem. Also set the generation timing of DR interrupt trigger (values set to bits 8 to 14 of the IT0CR and the IT1CR) (for example, the lead point of a public frame or self-station) to avoid the above problem.

4.3 Use of Mail Sending/Reception Function

This section describes the use of the MKY43 mail sending/reception function.

The CUnet protocol defines that a CUnet IC has all the mail sending/reception protocols. Mail sending/reception based on the CUnet protocol functions between CUnet ICs other than I/O station in the RUN phase.
At mail sending/reception by the MKY43, errors occur only on the sending, not on the receiving. Accordingly, the user system program can use the mail sending/reception function through the following basic operations and processing:

(1) Permission for mail reception
(2) Operation for mail reception
(3) Operation for mail sending and after completion of sending
(4) Operation against mail sending errors

The MKY43 has registers and user-support functions that help the above basic operations for mail sending and reception.

4.3.1 Permission for Mail Reception

The MKY43 has two mail receive buffers, MRB0 (Mail Receive Buffer 0) and MRB1 (Mail Receive Buffer 1) shown in ***"4.1.1 Memory Map"***. The MRB0 and MRB1 consist of 256 bytes each (Fig. 4.18).

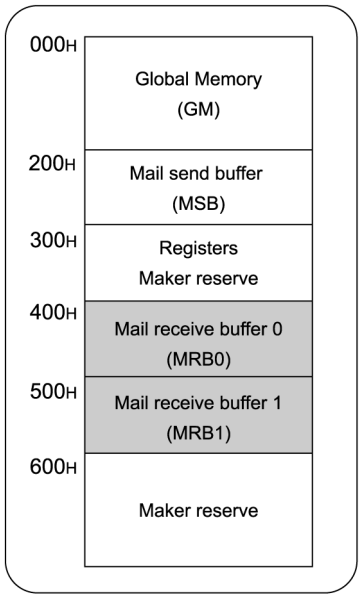


Fig. 4.18 Mail Receive Buffers

The MR0CR (Mail Receive 0 Control Register) permits the MRB0 to receive mail. The MR1CR (Mail Receive Control 1 Register) permits the MRB1 to receive mail (Fig. 4.19).

When the user system program writes "1" to bit 6 (RDY: ReaDY) of the MR0CR, the MRB0 is permitted to receive mail. The RDY bit returns to "0" upon mail reception. When "1" is written to bit 6 (RDY) of the MR0CR, the RCV (ReCeiVed) flag of bit 7, which indicates the completion of reception, changes to "0".

When the RDY bit of the MR0CR is "1", mail reception can be inhibited by writing "0" to this bit. However, writing "0" to this bit during mail reception is ignored and mail reception cannot be inhibited.
When the RDY bit or the RCV bit of the MR0CR is "1", the MRB0 is write-protected. If the MRB0 is read when the RDY bit of the MR0CR is "1", data is always "00H".

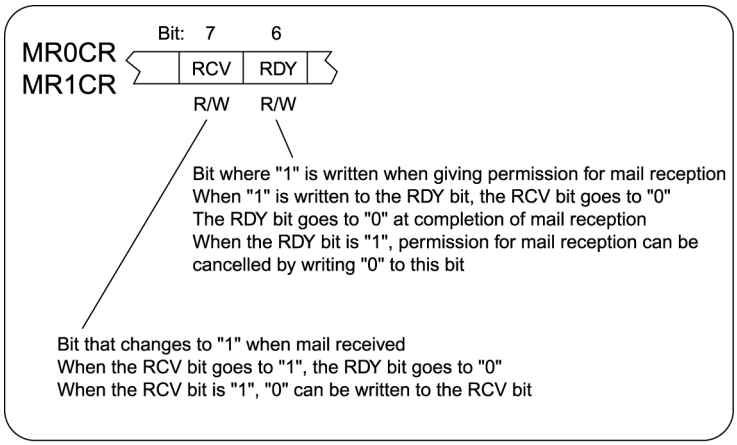

MR0CR
MR1CR
Bit: 7 6
RCV
RDY
R/W R/W
Bit where "1" is written when giving permission for mail reception
When "1" is written to the RDY bit, the RCV bit goes to "0"
The RDY bit goes to "0" at completion of mail reception
When the RDY bit is "1", permission for mail reception can be cancelled by writing "0" to this bit
Bit that changes to "1" when mail received
When the RCV bit goes to "1", the RDY bit goes to "0"
When the RCV bit is "1", "0" can be written to the RCV bit

Fig. 4.19 Permission for Mail Reception

When the user system program writes "1" to bit 6 (RDY) of the MR1CR, the MRB1 is permitted to receive mail. The RDY bit returns to "0" upon mail reception. When "1" is written to bit 6 (RDY) of the MR1CR, the RCV (ReCeiVed) flag of bit 7 in the MR1CR, which indicates the completion of reception, changes to "0".
When the RDY bit of the MR1CR is "1", mail reception can be inhibited by writing "0" to this bit. However, writing "0" to this bit during mail reception is ignored and mail reception cannot be inhibited.
When the RDY bit or the RCV bit of the MR1CR is "1", the MRB1 is write-protected. If the MRB1 is read when the RDY bit of the MR1CR is "1", data is always "00H".

Dataset received by mail is stored in the buffer with the RDY bit at "1". When both the RDY bits of the MR0CR and MR1CR are "1", received dataset is stored in the MRB0.

4.3.2 Operation for Mail Reception

When the datasets received by mail from other CUnet stations are stored in the MRB0, the MKY43 works as follows (Fig. 4.20):

(1) Causes bit 7 (RCV: ReCeiVed) of MR0CR to change to "1"
(2) Causes bit 6 (RDY: ReaDY) of MR0CR to change to "0"
(3) Stores dataset sizes (hexadecimal) received by mail in bits 0 to 5 (SiZe: SZ0 to SZ5) of MR0CR. The dataset sizes are given in 8 bytes as one unit.
(4) Stores source Station Addresses (SAs) (hexadecimal) in bits 8 to 13 (SRC: SouRCe0 to SouRCe5) of MR0CR
(5) Outputs interrupt triggers if mail reception interrupt triggers have been enabled.

The user system program must read datasets from the beginning of the MRB0, referring to the source SAs and dataset sizes from the MR0CR. "0" can be written to bit 7 (RCV) of the MR0CR.

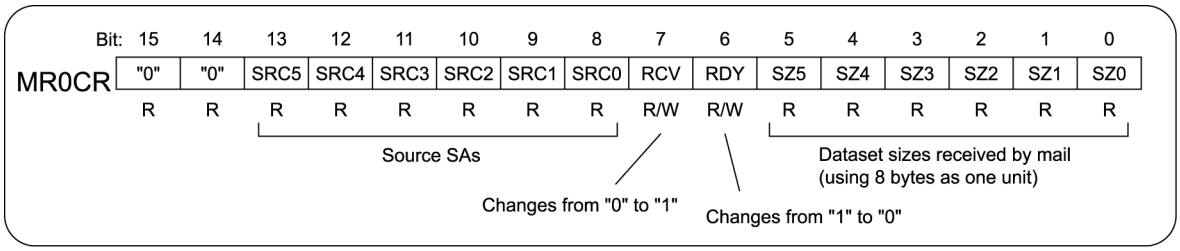

Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MR0CR
"0" "0" SRC5 SRC4 SRC3 SRC2 SRC1 SRC0 RCV RDY SZ5 SZ4 SZ3 SZ2 SZ1 SZ0
R R R R R R R R R/W R/W R R R R R R
Source SAs
Dataset sizes received by mail (using 8 bytes as one unit)
Changes from "0" to "1"
Changes from "1" to "0"

Fig. 4.20 MR0CR with Dataset Stored in MRB0

When the datasets received by mail from other CUnet stations are stored in the MRB1, the MKY43 works as follows (Fig. 4.21):

(1) Causes bit 7 (RCV: ReCeiVed) of MR1CR to change to "1"
(2) Causes bit 6 (RDY: ReaDY) of MR1CR to change to "0"
(3) Stores dataset sizes (hexadecimal) received by mail in bits 0 to 5 (SiZe: SZ0 to SZ5) of MR1CR. The dataset sizes are given in 8 bytes as one unit.
(4) Stores source Station Addresses (SAs) (hexadecimal) in bits 8 to 13 (SRC: SouRCe0 to SouRCe5) of MR1CR
(5) Outputs interrupt triggers if mail reception interrupt triggers have been enabled.

The user system program must read datasets from the beginning of the MRB1, referring to the source SAs and dataset sizes from the MR1CR. "0" can be written to bit 7 (RCV) of the MR1CR.

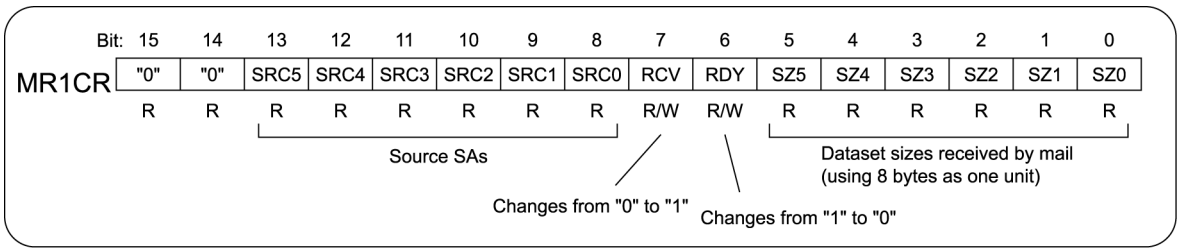

Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MR1CR
"0" "0" SRC5 SRC4 SRC3 SRC2 SRC1 SRC0 RCV RDY SZ5 SZ4 SZ3 SZ2 SZ1 SZ0
R R R R R R R R R/W R/W R R R R R R
Source SAs
Dataset sizes received by mail (using 8 bytes as one unit)
Changes from "0" to "1"
Changes from "1" to "0"

Fig. 4.21 MR1CR with Dataset Stored in MRB1

Even if the user system executes processing for the MRB0 after mail reception, the MKY43 can store dataset in the MRB1. Similarly, even if the user system executes processing for the MRB1 after mail reception, the MKY43 can also store dataset in the MRB0.

When the RCV bit of the MR0CR or MR1CR is "1", bit 6 (MR: Mail Received) of the SSR (System Status Register) also goes to "1". (The MR bit of the SSR is a flag bit where the "OR" of the "RCV bits of the MR0CR and MR1CR" is indicated.) The user system program can recognize mail reception by recognizing the MR bit of the SSR without recognizing the RCV bits of "MR0CR and MR1CR" individually.

For details of the function to output interrupt triggers when dataset is stored in the MRB0 or MRB1, refer to ***"4.5 Interrupt Trigger Generation Function"***.

(1) In the MKY43, if data is written to the RCV bit or RDY bit of the MR0CR, values of bits 0 to 5 (SiZe: SZ0 to SZ5) and bits 8 to 13 (SouRCe: SRC0 to SRC5), which are stored in the MR0CR, are cleared to "00H". This applies to the MR1CR similarly.

(2) The RDY bit of the MR0CR in the MKY43 can be operated when the START bit of the SCR is "1". In the MKY43, if the START bit of the SCR changes to "0" when the RDY bit of the MR0CR is "1", the RDY bit of the MR0CR also changes to "0". This applies to the RDY bit of the MR1CR similarly.

4.3.3 Operation for Mail Sending and after Completion of Sending

The MKY43 can mail the datasets written to the MSB (Mail Send Buffer) to one specific Station Address (SA). The procedure is shown below.

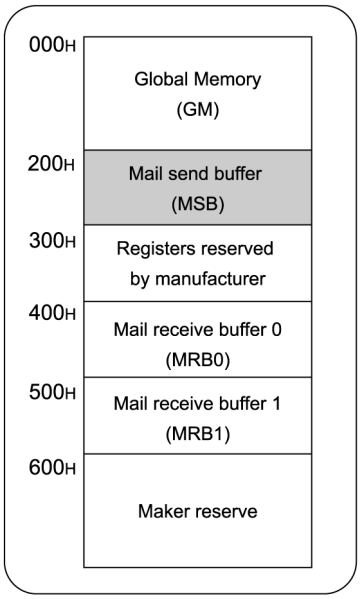


Fig. 4.22 Mail Send Buffer

(1) When the bit 14 (SEND) of MSCR (Mail Send Control Register) is "0", write the datasets sequentially from the starting address of the MSB (Fig. 4.22).

(2) Check that bit 15 (ERR: ERRor) of the MSCR is "0". If the ERR flag bit is not "0", the previous error remains. Set the flag bit to "0", referring to ***"4.3.4 Operation against Mail Sending Error"***. If the ERR flag bit is "1", writing "1" to the SEND bit described in (4) is ignored (Fig. 4.23).

(3) When setting the time-out of mail sending, write the time-out values (hexadecimals: "0004H to 1FFFH") defined by the user system using a cycle time as one unit to bits 0 to 12 (LiMit Time: LMT0 to LMT12) of the MSLR (Mail Send Limit time Register). The initial value of the MSLR is set to "1FFFH" by hardware reset. If the user system does not determine a time-out value, there is no need to write it. The data written to the MSLR is held until a hardware reset is activated and does not need to be set every mail sending.

(4) Write the dataset sizes (hexadecimal) to bits 0 to 5 (SiZe: SZ0 to SZ5) of the MSCR, the destination SAs (hexadecimal) to bits 8 to 13 (DeSTination: DST0 to DST5), and "1" to the SEND bit (bit 14). The dataset sizes are given in 8 bytes as one unit. For example, if a dataset is 34 bytes, its size is "05H". If a dataset is a maximum of 256 bytes, its size is "20H".

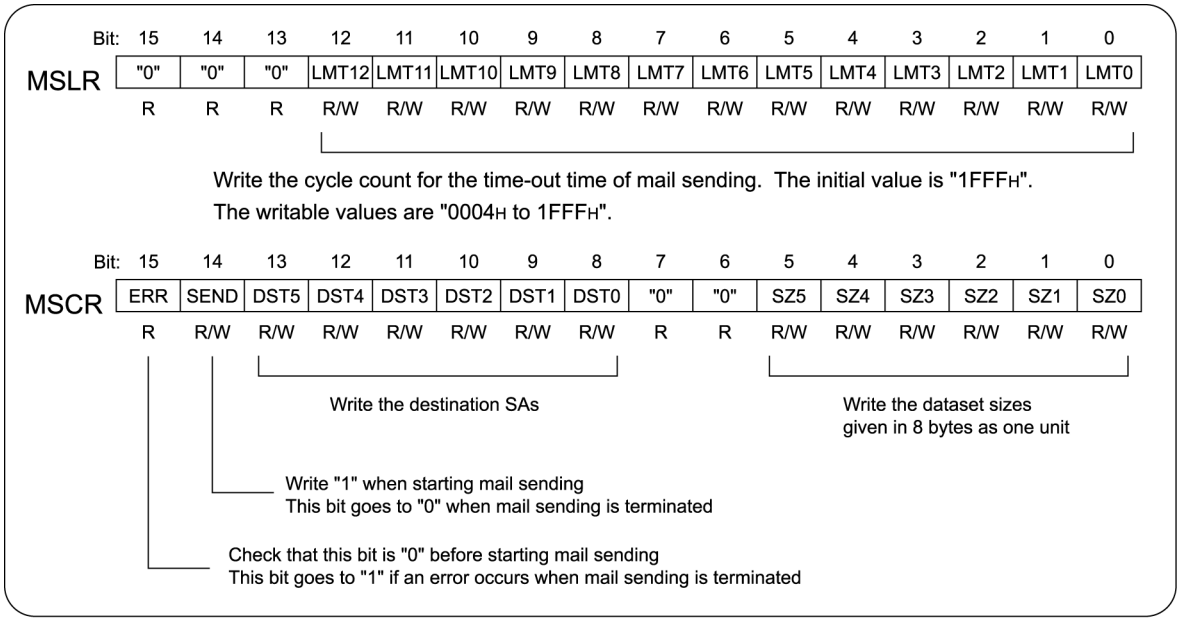

Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MSLR
"0" "0" "0" LMT12 LMT11 LMT10 LMT9 LMT8 LMT7 LMT6 LMT5 LMT4 LMT3 LMT2 LMT1 LMT0
R R R R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W
Write the cycle count for the time-out time of mail sending. The initial value is "1FFFH".
The writable values are "0004H to 1FFFH".
Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MSCR
ERR SEND DST5 DST4 DST3 DST2 DST1 DST0 "0" "0" SZ5 SZ4 SZ3 SZ2 SZ1 SZ0
R R/W R/W R/W R/W R/W R/W R/W R/W R R R/W R/W R/W R/W R/W R/W
Write the destination SAs
Write the dataset sizes
given in 8 bytes as one unit
Write "1" when starting mail sending
This bit goes to "0" when mail sending is terminated
Check that this bit is "0" before starting mail sending
This bit goes to "1" if an error occurs when mail sending is terminated

Fig. 4.23 Operation of MSLR and MSCR

(5) The MKY43 starts mail sending immediately after "1" is written to bit 14 (SEND) of the MSCR. The MSB is write-protected during mail sending. When the MSB is read during mail sending, data is set forcibly to "00H".

(6) Upon completion of mail sending, bit 14 (SEND) returns to "0". The completion of mail sending can be recognized by this bit transition.
The MKY43 can output interrupt triggers by the completion of mail sending. For details, refer to ***"4.5 Interrupt Trigger Generation Function"***.

(7) Check bit 15 (ERR) of the MSCR after the completion of mail sending.
If the ERR flag bit is "0", mail sending is completed correctly. This assures that the MKY43 was able to send datasets to the mail receive buffers at a destination station.
If the ERR flag bit is "1", the user system program needs to refer to ***"4.3.4 Operation against Mail Sending Error"*** and deal with accordingly.
When referring to the time required for mail sending (time taken from when sending is started until it is completed) by the user system program, read the Mail Send Result Register (MSRR).
The MKY43 stores the number of cycles required from when mail sending is started until it is completed to the MSRR when mail sending is completed. The MSRR holds this value until the next mail sending is completed or a hardware reset is activated (Fig. 4.24).

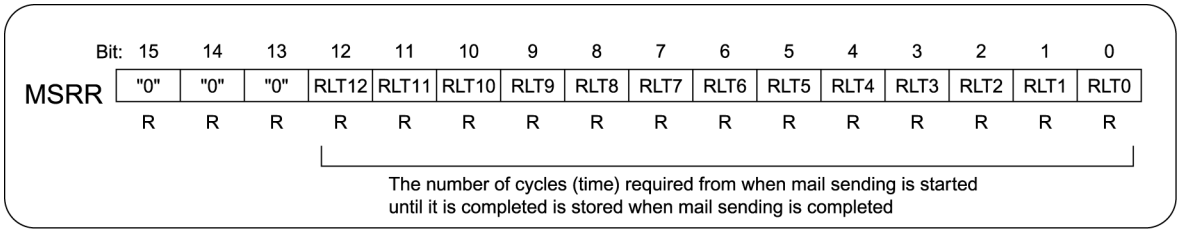

Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MSRR
"0" "0" "0" RLT12 RLT11 RLT10 RLT9 RLT8 RLT7 RLT6 RLT5 RLT4 RLT3 RLT2 RLT1 RLT0
R R R R R R R R R R R R R R R R
The number of cycles (time) required from when mail sending is started
until it is completed is stored when mail sending is completed

Fig. 4.24 MSRR

4.3.4 Operation against Mail Sending Errors

The procedure and quality for mail sending/reception are strictly managed by the CUnet protocol of the MKY43. Therefore a mail sending error exists only on the sending, not on the receiving. There are several types of mail sending errors as follows:

(1) NORDY (destination NOt ReaDY): Mail sending failed because a mail receive buffer at a destination CUnet station is not in the RDY state.
(2) NOEX (destination NOt EXist): Mail sending failed because a destination CUnet station is not connected to a network or is in a phase other than RUN.
(3) TOUT (limit Time OUT): Mail sending could not be completed within the cycle time set in the MSLR (Mail Send Limit time Register).
(4) SZFLT (SiZe FauLT): Mail sending failed because the sizes (hexadecimal) of datasets set in bits 0 to 5 (SiZe: SZ0 to SZ5) of the MSCR (Mail Send Control Register) are invalid.
(5) LMFLT (LiMit time FauLT): Mail sending failed because the values (hexadecimal) set in bits 0 to 12 (Limit Time: LT0 to LT12) of the MSLR (Mail Send Limit time Register).
(6) STOP (communication STOPped): A self-station changed to a phase other than RUN during mail sending and mail sending stopped.

If mail sending is unsuccessful, the MKY43 stores the status with error type "1" in the MESR (Mail Error Status Register) (Fig. 4.25).
When any of bits 0 to 5 of the MESR are "1", both bit 15 (ERR: ERRor) of the MSCR and bit 7 (MSE: Mail Send Error) of the SSR (System Status Register) are set to "1". If mail sending is unsuccessful, the user system program needs to refer to the MESR and deal with in accordance with the error type. Bits 0 to 5 of the MESR can all be cleared to "0" by writing some data to addresses where they exist. This clearing causes both bit 15 (ERR) of the MSCR and bit 7 (MSE) of the SSR to return to "0".

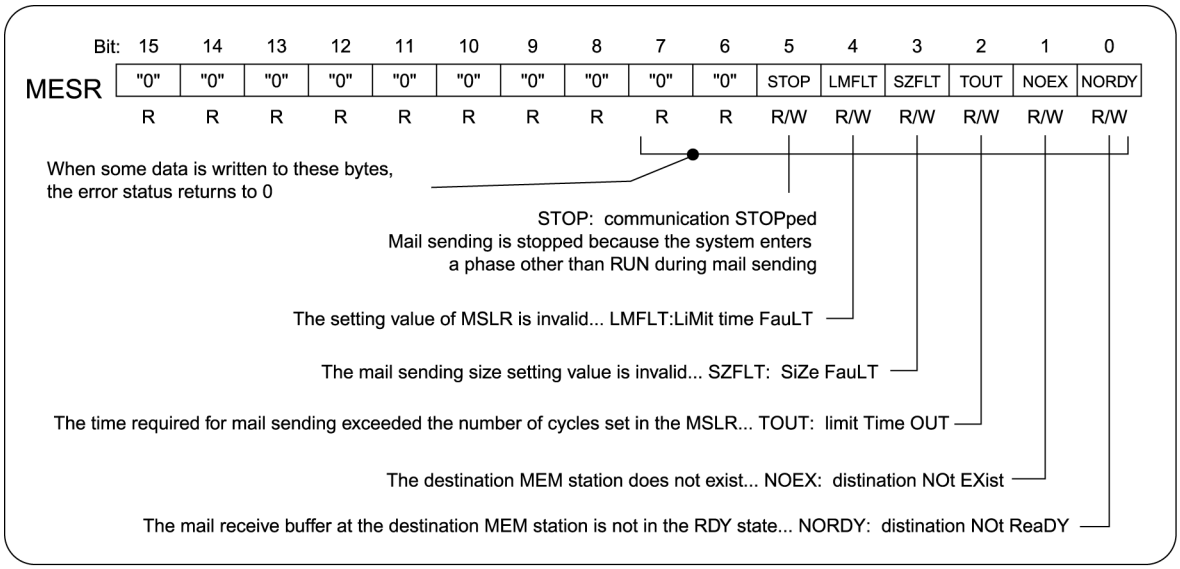

Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MESR
"0" "0" "0" "0" "0" "0" "0" "0" "0" "0" STOP LMFLT SZFLT TOUT NOEX NORDY
R R R R R R R R R R R/W R/W R/W R/W R/W R/W
When some data is written to these bytes, the error status returns to 0
STOP: communication STOPped
Mail sending is stopped because the system enters a phase other than RUN during mail sending
The setting value of MSLR is invalid... LMFLT:LiMit time FauLT
The mail sending size setting value is invalid... SZFLT: SiZe FauLT
The time required for mail sending exceeded the number of cycles set in the MSLR... TOUT: limit Time OUT
The destination MEM station does not exist... NOEX: distination NOt EXist
The mail receive buffer at the destination MEM station is not in the RDY state... NORDY: distination NOt ReaDY

Fig. 4.25 MESR

4.3.5 Quality Assurance for Mail Sending/Reception

If trouble with sending packet by mail occurs due to environmental problems including external noise, the MKY43 with the CUnet protocol is recovered by resending (retry). Resending is executed three times.
If packets cannot be sent by mail even after resending is executed three times, processing is terminated with an NOEX (destination NOt EXist) error. This prevents the mail or the datasets becoming lost in transit.
Datasets sent/received by mail are quality-guaranteed as with packet that shares memory data. This prevents data errors that are likely to occur.

Reference In the CUnet protocol, even if retry (resending) occurs in mail sending, it never affects memory data sharing.

4.3.6 User-support Functions in Mail Sending/Reception

In a CUnet, two CUnet stations can send/receive mail simultaneously.
For example, mail from the MEM station with SA = 1 to the MEM station with SA = 2 and mail from the MEM station with SA = 3 to the MEM station with SA = 4 can be sent/received simultaneously. However, if mail sending from the MEM station with SA = 3 to the MEM station with SA = 1 are started immediately after mail sending from the MEM station with SA = 2 to the MEM station with SA = 1 were started, since the destination is same, the mail sending from the MEM station with SA = 3 to the MEM station with SA = 1 are kept waiting during mail sending from the MEM station with SA = 2 to the MEM station with SA = 1.

The CUnet has a function to control priority assigned when multiple mail sendings are started simultaneously.
In the CUnet, if three or more mail sendings are started simultaneously, priority is given to a mail sending from a smaller value Station Address (SA). This priority is rotated. Therefore, even if the CUnet station with a small value SA performs mail sending continuously, mail sending from the MKY43 with a large value SA are not kept endlessly waiting.

4.3.7 Estimation of Mail Sending/Reception Time

The estimated time required for mail sending/reception of the MKY43 can be calculated using Equation 4.3. It does not include the waiting time taken when two or more CUnet stations start mail sending/reception simultaneously and the resending (retry) time when a delay occurs in packet transmission. Therefore, use the time calculated using Equation 4.3 as a guide when building up a user system.

Equation 4.3 (((Byte count of dataset + 7) ÷ 8) + 3) × cycle time [s]

In a partial solution (underlined part), digits after the decimal point are dropped.

Reference For example, in a system (FS = 3) that is operated by four CUnet stations with a baud rate of 12 Mbps, the time required for sending/receiving of 250 bytes of mail can be calculated as follows:
(((250 + 7) ÷ 8) + 3) × 109 μs = 35 × 109 μs = 3.82 ms

4.3.8 Precautions for Mail Sending/Reception

Note the following when the user system uses the MKY43 mail sending/reception function:

(1) Mailing is limited to a station in the MEM mode.
The address of the IO station or the Station Address (SA) owned and expanded by OWN setting cannot be specified as a mailing address. If the address of the IO station is specified accidentally, the mail to that address is terminated with an NORDY (destination NOt ReaDY) error. If the SA owned and expanded by the OWN setting is specified accidentally, the mail to that SA is terminated with an NOEX (destination NOt EXist) error.

(2) Broadcast mailing (a method called "discharge" used for general RS-232C or "broadcast" in LAN communication) cannot be performed.

(3) Mail sending and reception is performed in 8 bytes.

Mail sending/reception by the MKY43 guarantees both sending success and data quality by the CUnet protocol. Therefore, broadcast mailing that cannot be guaranteed by the MKY43 protocol cannot be used.

4.4 Detailed Operation and Management of CUnet System

The user system program can operate the MKY43 to operate and manage details of a CUnet system as shown below:

(1) Monitoring before network start
(2) Resizing of cycle time
(3) Detection and handling of CUnet station in BREAK phase
(4) Detection and handling of jammer
(5) Controling and monitoring network quality
(6) PING instruction
(7) Function to detect mode of each station
(8) GMM (Global Memory Monitor) function
(9) Frame option [for HUB]

4.4.1 Monitoring before Network Start

The MKY43 receives packets from other CUnet stations even before network start (at START bit of SCR "0"). Global memory updating and mail reception are not performed with the received packets, but updating of the Receive Flag Register (RFR) and Final Station Register (FSR) and synchronization with and calibration of other CUnet stations in cyclic time-sharing are performed. This enables the user system program to perform monitoring before network start as shown below:

(1) The user system program can recognize that a resized cycle is operating on a network. A resized cycle is operating if values stored in bits 0 to 5 (FS0 to FS5) of the FSR are anything other than the initial value 63 (3FH). If an FSR value is smaller than the owned area of a self-station, the user system program can also estimate that the MKY43 enters the BREAK phase after having started the self-station network.

(2) The user system program can recognize the Station Time (ST) that is the operation timing in cyclic time sharing by reading bits 0 to 6 (ST0 to ST6) of the SCR (System Control Register).

(3) At the timing that the Station Time (ST) exceeds the value stored in the FSR (at the public-frame period), by reading the RFR, the user system program can recognize that if there is a bit at "1" in any place other than the owned area of a self-station, the CUnet station with the station address corresponding to that bit is operating on the network.

When other CUnet stations are not in operation, the ST that can be obtained in (2) above is in the free-running state and is not synchronized with other CUnet stations.

The ST that can be obtained in (2) above can be used to recognize the timing both after and before the network starts.

4.4.2 Resizing of Cycle Time

The MKY43 can perform resizing defined in “Increased Practicality” in the CUnet protocol.
In a CUnet consisting of the MKY43 with the CUnet protocol, the initial value of a Final Station (FS) is 63 (3FH). Resizing is useful when 64 frames are not needed in the user system. For example, in a user system using only two CUnet stations with SA = 0 and SA = 1, a large network is not in use during the Station Time (ST) with SA = 2 to 63 constituting a cycle. In this case, changing the FS value to “1” provides the most efficient cycle. For example, in operation at 12 Mbps, the response time of memory data sharing increases from 2.365 ms to 102 μs (Fig. 4.26).

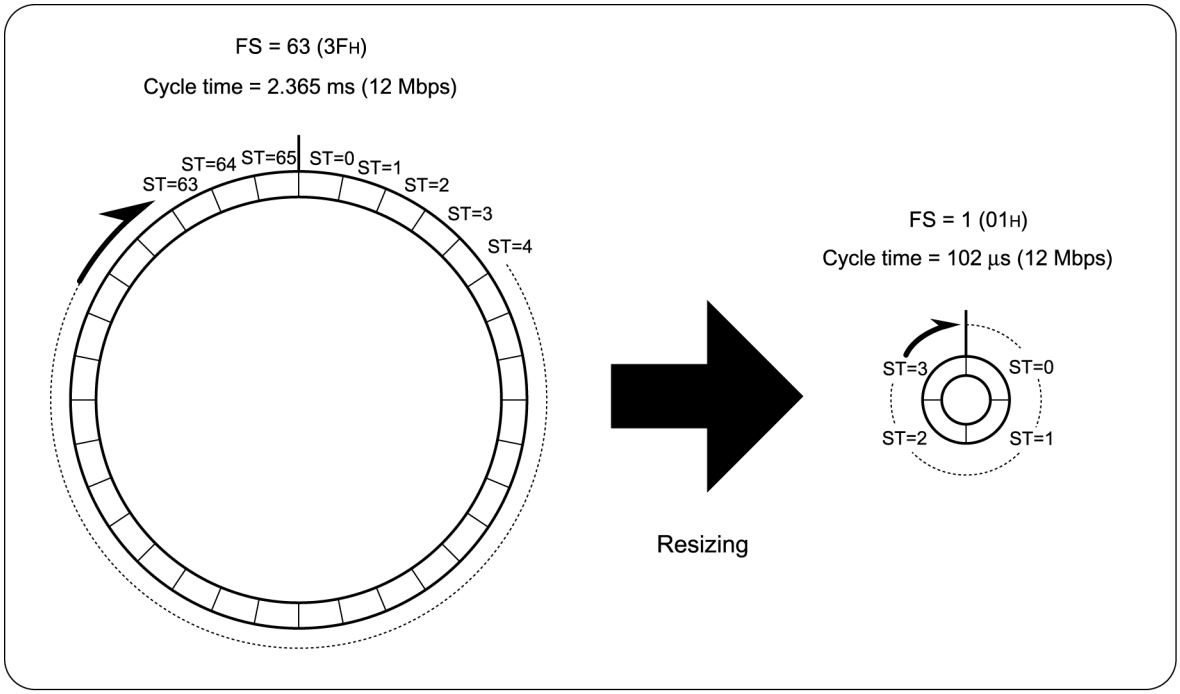


Fig. 4.26 Resize

4.4.2.1 Resizing

Resizing is performed when the user system program writes a new Final Station (FS) value to the New Final Station Register (NFSR). It may be affected by rejection of values to be written to the NFSR or correlation with other CUnet stations. To prevent this problem, when resizing, follow the procedures below (Fig. 4.27):

(1) Write a value to bits 0 to 5 (NFS0 to NFS5) of the NFSR.

(2) Read the NFSR to check that the written value is stored in the register. If the value is not stored in the register, the register is not ready or the value is rejected. Refer to ***"4.4.2.2 Rejection of Resizing"*** to stop resizing or perform resizing again with an appropriate value.

(3) Wait until the NFSR value changes to "00H". When the NFS bit finishes sending the resizing instruction to the communication line four times, the NFSR value changes to "00H".

(4) Read the System Status Register (SSR) to check that bit 8 (RO: Resize Overlap) of the SSR is "0". If the RO bit is "1", refer to ***"4.4.2.3 Resize Overlap (RO)"*** and ***"4.4.2.4 Caution when RO Occurs"*** to deal with accordingly.

(5) Read the System Control Register (SCR) to check that the bit 9 (RUN) is "1". If the Run bit of the read SCR is "0", refer to ***"4.1.8 Network Stop"*** to deal with accordingly.

(6) Read the Final Station Register (FSR) to check that its value is the same as the value written to the NFSR. If the value is different, perform resizing again from the beginning (from step (1)).

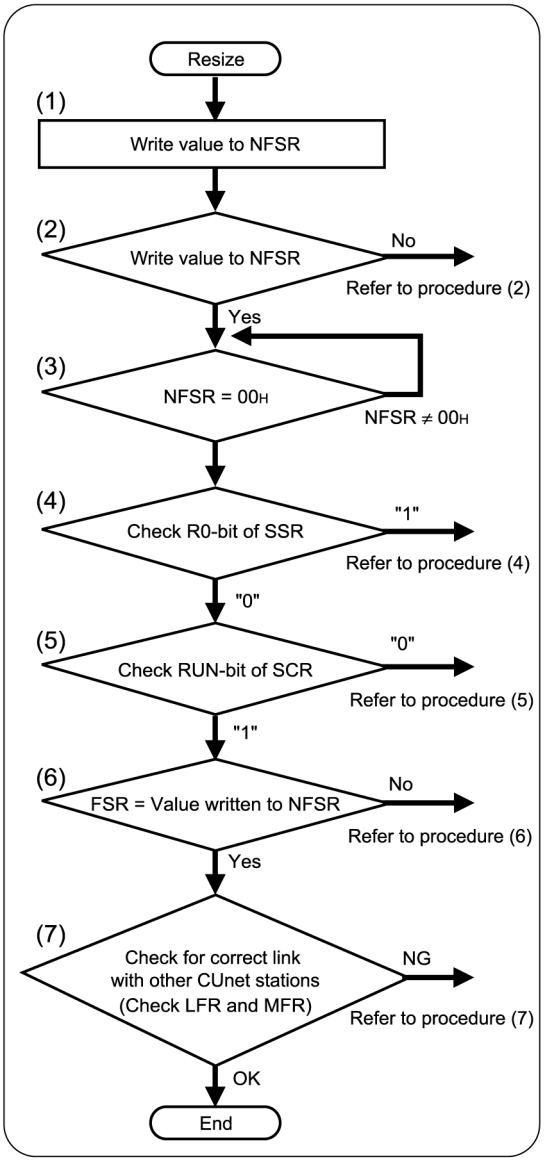


Fig. 4.27 Resizing

(7) If, on the network, there is a CUnet station stopped by Out of Cycle (OC) due to reception of the resizing, the bits of the Link Flag Register (LFR) and Member Flag Register (MFR) corresponding to the CUnet station change from their pre-resizing status within the elapse of several cycle times.

Use the LFR, MFR, and function to monitor them described in ***"4.2.3 Quality Assurance of GM Data"*** to check that the link with other CUnet stations required by the user system is correct.

If the link is incorrect, refer to ***"4.1.8 Network Stop"*** (particularly, Stop by OC) to perform expanded resizing and promote entry of a stopped CUnet station.

When any "one" of the CUnet stations performs resizing, the Final Station (FS) values of all CUnet stations connected to the network are updated to resized values. In this case, MEM stations other than the station that performed resizing can output interrupt triggers when the FS values are updated. For details, refer to ***"4.5 Interrupt Trigger Generation Function"***.

The cycle time during the period where the NFSR value is not "00H" does not conform to Equation 4.2 (refer to ***"4.1.6 Cycle Time of CUnet"***).

Resizing can be performed from any MEM station (but cannot be executed from the I/O station).

For the resizing in the MKY40, the NFSR value does not return to "00H" automatically. So, note that the resizing in the MKY40 is different from that in the MKY43.

4.4.2.2 Rejection of Resizing

At resizing, writing to the NFSR is rejected in the following cases:

(1) The NFSR is write-protected when the MKY43 is not in the RUN phase.

(2) The NFSR is write-protected when a value excluding the owned area of a self-station is written. For example, if a self-station is set at "SA = 2 and OWN = 5", its owned area range is from "02H to 06H" and values more than "06H" can be written. However, values less than "05H" exclude the owned area and are rejected.

The MKY43 avoids contradictions in CUnet operation using these write-protection method.

4.4.2.3 Resize Overlap (RO)

However, when multiple MEM stations perform resizing concurrently, priority is given to the resizing instruction of the MEM station with a smaller value SA. The MEM station, which received a priority resizing instruction while New Final Station Register (NFSR) is storing the value to be resized, changes bit 8 (Resize Overlap: RO) of the SSR to "1" and warns the user system program about a resize overlap.

The occurrence of the resize overlap reveals that the algorithm of the user system itself is contradictory. Optimize the system algorithm. The warning about the resize overlap (RO bit of the SSR is "1") can be cleared to "0" when the user system program writes "1" to the same bit (RO bit of SSR) (Fig. 4.28).

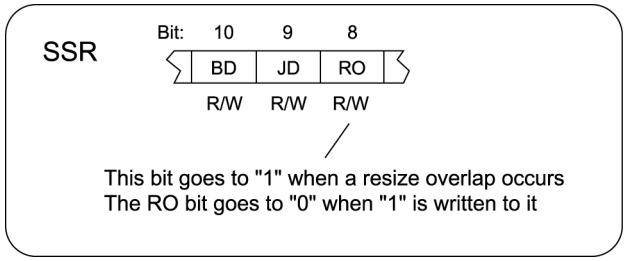


Fig. 4.28 RO Bit of SSR

When the bit 8 (RO) of the SSR changes to "1", the MKY43 can output interrupt triggers. Also, note that, for the RO which occurs while the bit 8 (RO) of the SSR is "1", the interrupt does not occur. For details, refer to ***"4.5 Interrupt Trigger Generation Function"***.

Caution If both the Resize Overlap (RO) interrupt and Resize Complete (RC) interrupt have been enabled when a resize overlap occurs, both the RO interrupt and RC interrupt occurs simultaneously.

4.4.2.4 Caution when RO Occurs

If a resize overlap occurs, it is hard to specify the FS value to be resized depending on the operation timing and the resizing instruction priority of an MEM station. To prevent these problems, use an algorithm to prevent the occurrence of resize overlaps as described in the following examples:

(1) Specify one MEM station to perform resizing.
(2) The user system where multiple MEM stations perform resizing should hold a superordinate concept (program) requiring acquisition of the right to perform resizing.

4.4.3 Detection and Handling of CUnet Station in BREAK Phase

The MKY43 may enter the BREAK phase:

- When the CUnet station with an owned area larger than a Final Station (FS) value starts the network in the cycle that the FS value is resized as described in ***"4.4.2 Resizing of Cycle Time"***
- When the CUnet station stopped by OC (Out of Cycle) described in ***"4.1.8.2 Details of OC (Out of Cycle)"*** starts the network again

The CUnet station in the BREAK phase issues a break packet to another CUnet station in the stage of public frames constituting a cycle. The MKY43 receives this break packet and then set bit 10 (BD: Break Detect) of the System Status Register (SSR) to "1" to warn the user system program about the presence of a CUnet station in the BREAK phase (Fig. 4.29).

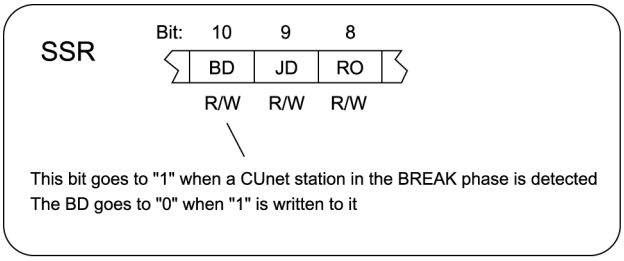

SSR
Bit: 10 9 8
BD JD RO
R/W R/W R/W
This bit goes to "1" when a CUnet station in the BREAK phase is detected
The BD goes to "0" when "1" is written to it

Fig. 4.29 BD Bit of SSR

When bit 10 (BD) of the SSR changes to "1", the MKY43 can output an interrupt trigger. Also, note that, for the BD which occurs while the bit 10 (BD) of the SSR is "1", the interrupt does not occur. For details, refer to ***"4.5 Interrupt Trigger Generation Function"***.

Bit 10 (BD) can be cleared by writing "1". It changes to "1" again when a break packet is received subsequently.

Perform expanded resizing to change FS values through operation in ***"4.4.2 Resizing of Cycle Time"*** when the user system program that recognized the presence of a CUnet station in the BREAK phase by receiving interrupt triggers or by reading the SSR to check that the BD bit is "1" adds the CUnet station in the BREAK phase to a cycle.

Reference The station address and owned width of the CUnet station in the BREAK phase are unidentified for a MEM station that performs expanded resizing. Therefore, perform expanded resizing to the maximum FS value "63 (3FH)".

4.4.4 Detection and Handling of Jammer

When a jammer (CUnet station that can only send a packet due to hardware trouble or failure) is detected, the CUnet protocol defines that the MKY43 warns the user system about the jammer.
When a jammer is detected, the MKY43 sets bit 9 (JD: Jammer Detect) of the SSR to "1" and warns the user system program about it (Fig. 4.30).

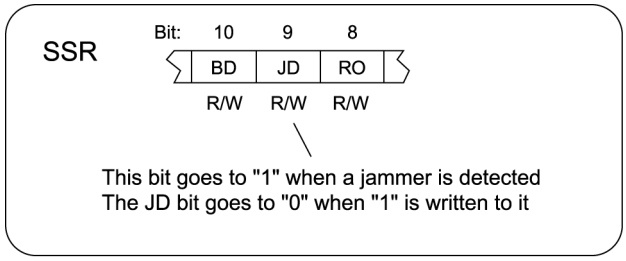


Fig. 4.30 JD Bit of SSR

Bit 9 (JD) of the SSR can be cleared by writing "1". It changes to "1" again when a jammer is detected subsequently.

When bit 9 (JD) of the SSR goes to "1", the MKY43 can output interrupt triggers. Also, note that, for the JD which occurs while the bit 9(JD) of the SSR is "1", the interrupt does not occur. For details, refert to ***"4.5 Interrupt Trigger Generation Function"***.

The user system program that recognized the jammer by reading the SSR to check that the JD bit is "1" warns the user system operator or manager to remove the jammer or perform failure recovery.

Even if no CUnet stations have a hardware failure, a slight difference in the start timing may occasionally cause a jammer to be detected at network start. Therefore, if the JD bit is "1", clear the bit and check for a jammer at network start and then issue a warning to an operator or manager.

Reference Because the CUnet station with a jammer cannot receive a packet, the jammer on the network cannot be removed forcibly. Consequently, the jammer must either be removed by an operator or manager, or failure recovery must be performed.

4.4.5 Controling and Monitoring Network Quality

The MKY43 has two concepts, LCARE (Link CARE) and MCARE (Member CARE) that can control network quality. It also has the #MON (MONitor) pin that can monitor the state that a link with other CUnet stations is stable. In understanding this section, refer to ***"4.2.3 Quality Assurance of GM Data"***.

4.4.5.1 LCARE Signal Output

A dead link defined in the CUnet protocol does not occur in a stable CUnet operating environment. It occurs when "CUnet station disconnects", when "trouble with receiving or sending packet occurs due to environmental problems including external noise" or when "a network has marginal performance". Therefore, it is possible to identify what caused a dead link, except when a CUnet station is disconnected intentionally by the user system. Network hardware and environmental quality can be recognized by controlling the occurrence of this dead link; the dead link is called "LCARE".

When LCARE occurs, the MKY43 outputs pulse signals that go Low for a given time from the #LCARE pin, regardless of the bit status stored in the LGR described in ***"4.2.3.3 Link Group Register (LGR)"***. The occurrence of LCARE can be checked visually by connecting an LED indicator to the #LCARE pin. For details of connecting the LED indicator, refer to ***"3.7 Connecting LED Indication Pins"***.

Up to 255 LCARE occurrences are indicated by bits 0 to 7 (LCC0 to LCC7) of the Care Counter Register (CCR) (Fig. 4.31). LCC of the CCR is held as "255 (FFH)" LCARE occurrences without counting more than 256 times.
When recognizing the number of LCARE occurrences with the user system program, read bits 0 to 7 (LCC0 to LCC7) of the CCR.

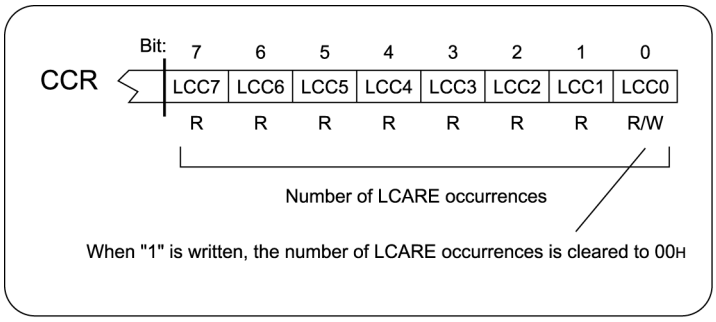

Bit: 7 6 5 4 3 2 1 0
CCR
LCC7 LCC6 LCC5 LCC4 LCC3 LCC2 LCC1 LCC0
R R R R R R R R/W
Number of LCARE occurrences
When "1" is written, the number of LCARE occurrences is cleared to 00H

Fig. 4.31 Number of LCARE Occurrences of CCR

When clearing the number of LCARE occurrences by the user system program, write "1" to bit 0 of the CCR.

A Low pulse output from the #LCARE pin is generated by a retriggerable one-shot multivibrator with a minimum time of "2505728 × TXI". Therefore, if a new dead link occurs within this time, the Low pulse width gets longer. If the driving clock of the MKY43 is 48 MHz, the minimum time of the Low pulse is about 52 ms and the lit LED can be seen.

Caution LCARE occurs and Low pulses are output from the #LCARE pin even when resizing described in ***"4.4.2 Resizing of Cycle Time"*** disables a link with the CUnet station with which the link has been established.

4.4.5.2 MCARE Signal Output

In a CUnet, "dead link" occurs consecutively three times in the same CUnet station "when a CUnet station disconnects", "when a system is in a poor operating environment", and "when a network has marginal performance". In the MKY43, the occurrence of three consecutive dead links is controlled by the MFR described in ***"4.2.3.5 Member Flag Register (MFR)"*** and is considered to be "Member decrease" described in ***"4.2.3.7 Detection of Member Increase and Decrease"***.
"Member decrease" is also called "MCARE (Member CARE)".
The MKY43 outputs pulse signals that go Low for a given time from the #MCARE pin, regardless of the bit status stored in the MGR described in ***"4.2.3.6 Member Group Register (MGR)"***. The occurrence of MCARE can be checked visually by connecting an LED indicator to this #MCARE pin. For details of connecting the LED indicator, refer to ***"3.7 Connecting LED Indication Pins"***.

It is possible to identify what caused MCARE; "when a system is in an extremely bad environment" or "when a network has marginal performance", except "when a CUnet station is disconnected intentionally by the user system". Network hardware and environmental quality can be recognized by controlling the occurrence of the MCARE.

Up to 255 MCARE occurrences are indicated at bits 8 to 15 (MCC0 to MCC7) of the Care Counter Register (CCR) (Fig. 4.32). MCC of the CCR is held at "255 (FFH)" MCARE occurrences without counting more than 256 times.
When recognizing the number of MCARE occurrences with the user system program, read bits 8 to 15 (MCC0 to MCC7) of the CCR.

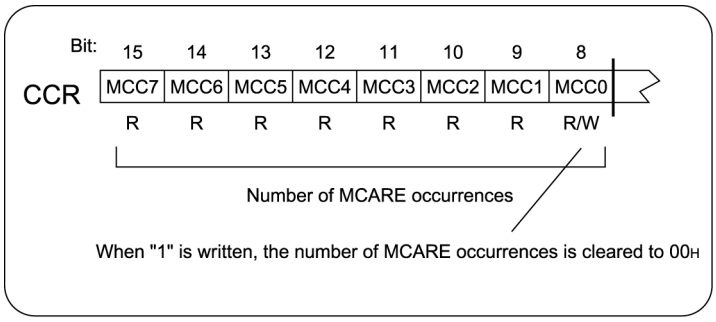

Bit: 15 14 13 12 11 10 9 8
CCR
MCC7 MCC6 MCC5 MCC4 MCC3 MCC2 MCC1 MCC0
R R R R R R R R/W
Number of MCARE occurrences
When "1" is written, the number of MCARE occurrences is cleared to 00H

Fig. 4.32 Number of MCARE Occurrences of CCR

When clearing the number of MCARE occurrences by the user system program, write "1" to bit 8 of the CCR.
A Low pulse output from the #MCARE pin is generated by a retriggerable one-shot multivibrator with a minimum time of "2505728 × TXI". Therefore, if a new MCARE occurs within this time, the Low pulse width gets longer. If the driving clock of the MKY43 is 48 MHz, the minimum time of the Low pulse is about 52 ms and lit LED can be seen.

Caution MCARE occurs and Low pulses are output from the #MCARE pin even when resizing described in ***"4.4.2 Resizing of Cycle Time"*** disables a link with the CUnet station with which the link has been established.

4.4.5.3 MON Signal Output

If a link is established consecutively more than three times, the MKY43 considers the link with other stations to be stable. This status is controlled by the Member Flag Register (MFR) described in ***"4.2.3.5 Member Flag Register (MFR)"***. The MKY43 outputs a Low level to the #MON pin when "1" is stored in any of the bits corresponding to CUnet stations other than the self-station of the MFR and outputs a High level in any other status (Fig. 4.33). The 'stable status of a link with other CUnet stations' can be checked visually by connecting an LED indicator to the #MON pin so that it can go ON when a Low level is output. For details of connecting the LED indicator, refer to ***"3.7 Connecting LED Indication Pins"***.

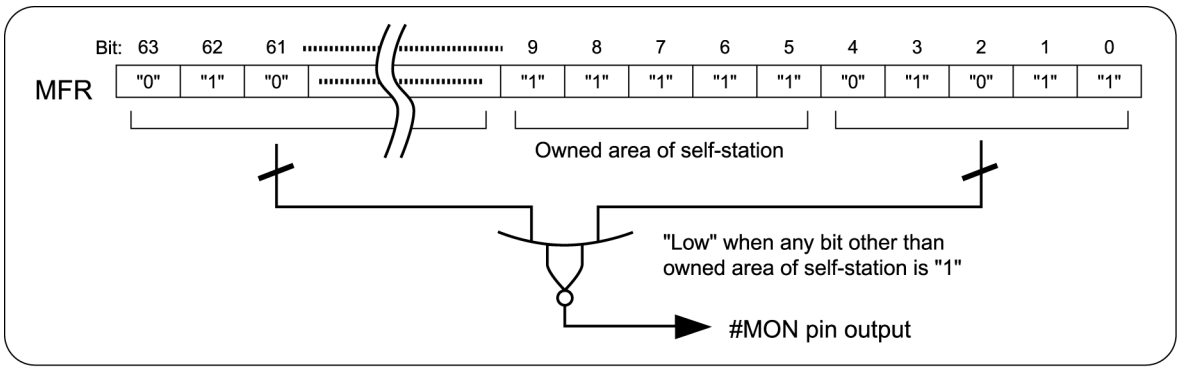

Bit: 63 62 61 9 8 7 6 5 4 3 2 1 0
MFR
"0" "1" "0" "1" "1" "1" "1" "1" "0" "1" "0" "1" "1"
Owned area of self-station
"Low" when any bit other than
owned area of self-station is "1"
#MON pin output

Fig. 4.33 Example of Output to #MON Pin

Caution If the MKY43 stops by OC (Out of Cycle), the status of the MFR may be hold and therefore a Low level to the #MON pin may continue to be output. When network stop by OC occurs in the MKY43, the user system program must perform processing based on ***"Appendix 3 Processing when Network Stop by OC (Out of Cycle) Occurs"***.

4.4.6 PING Instruction

The MKY43 in the RUN phase can issue the PING instruction to another CUnet station connected to the network.
The PING signal inside the MKY43 is kept High after hardware reset.
The MKY43 that received the PING instruction from the network changes the level of the internal PING signal to "Low".
The MKY43 that received packets other than the PING instruction from the network changes the level of the internal PING signal to "High".

The PING signal inside the MKY43 can be output to the UTY1 (UTilitY1) pin (pin 51) and the UTY2 (UTilitY2) pin (pin 54) by setting the UTCR (UTility pin Control Register). For the UTCR setting, refer to ***"3.8 Connection of UTY1 Pin and UTY2 Pin"***.

When an interrupt trigger is enabled by receiving the PING instruction, the interrupt trigger can also be output from the MKY43 to a user CPU when the MKY43 receives the PING instruction. For details, refer to ***"4.5 Interrupt Trigger Generation Function"***.

What to use the PING signal output to the UTY1 pin and UTY2 pin is not specified in the CUnet protocol and can be defined freely by the user system. For example, this signal can be used to reset a user CPU when it runs away.

In the MKY43, to issue the PING instruction to another CUnet station connected to a network, proceed as follows (Fig. 4.34):

(1) Write the destination Station Address (SA) of the PING signal to bits 0 to 5 (Target Station: TS0 to TS5) of the Query Control Register (QCR) and "1" to bit 7 (PING).
(2) When the PING instruction is issued to a network, bit 7 (PING) returns to "0".

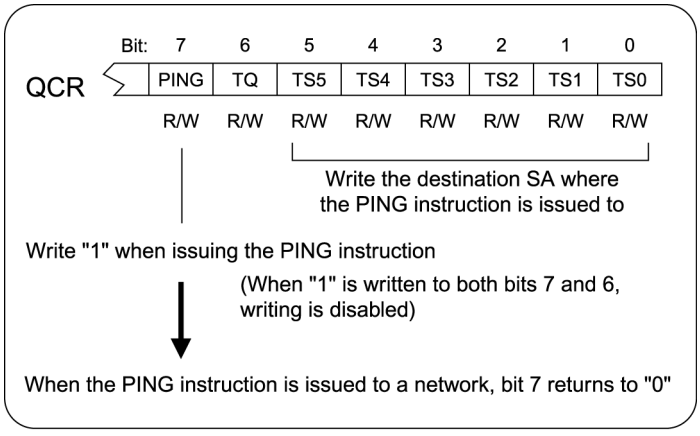

Bit: 7 6 5 4 3 2 1 0
QCR
PING TQ TS5 TS4 TS3 TS2 TS1 TS0
R/W R/W R/W R/W R/W R/W R/W R/W
Write the destination SA where the PING instruction is issued to
Write "1" when issuing the PING instruction
(When "1" is written to both bits 7 and 6, writing is disabled)
When the PING instruction is issued to a network, bit 7 returns to "0"

Fig. 4.34 Issuing PING Instruction

Caution The PING instruction can also be issued even to the SA of a CUnet station that does not exist on the network. However, the transition and the output to the pin of the target PING signal are not guaranteed.

4.4.7 Function to Detect Mode of Each Station

Operating the QCR of the MKY43 enables the user system to recognize the current mode of each CUnet station corresponding to SAs based on the type codes shown in Table 4-2.

To check the mode of other CUnet station connected to a network, proceed as follows (Fig. 4.35):

(1) Write the target station addresses to bits 0 to 5 (Target Station: TS0 to TS5) of the QCR and "1" to bit 6 (TQ: Try Query).

(2) At completion of checking, bit 6 (TQ) returns to "0" and type codes shown in Table 4-2 are stored in bits 8 to 12 (Station Type: ST0 to ST4).

(3) Use the user system program to read the QCR and check that bit 6 (TQ) is "0", and obtain the type codes from bits 8 to 12 (ST0 to ST4).

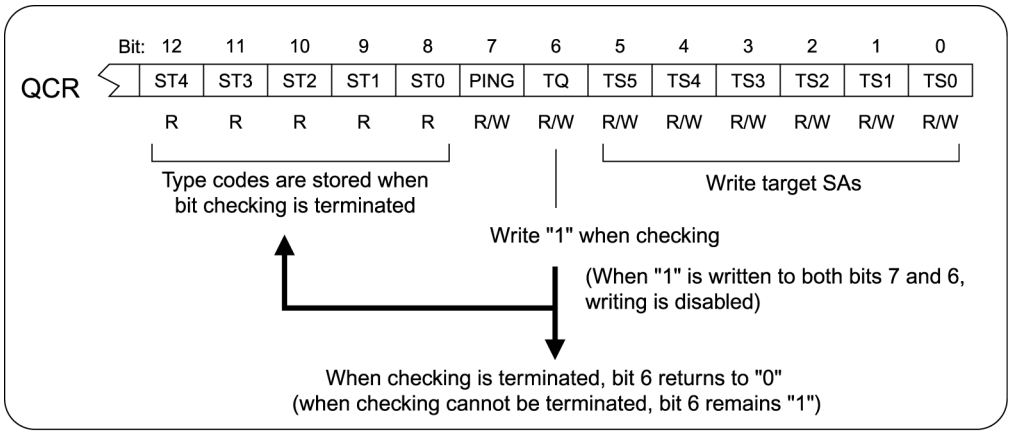

Bit: 12 11 10 9 8 7 6 5 4 3 2 1 0
QCR
ST4 ST3 ST2 ST1 ST0 PING TQ TS5 TS4 TS3 TS2 TS1 TS0
R R R R R R/W R/W R/W R/W R/W R/W R/W R/W
Type codes are stored when bit checking is terminated
Write target SAs
Write "1" when checking
(When "1" is written to both bits 7 and 6, writing is disabled)
When checking is terminated, bit 6 returns to "0"
(when checking cannot be terminated, bit 6 remains "1")

Fig. 4.35 Mode Checking for Each MEM Station

If the target CUnet station is not on the network, bit 6 (TQ) does not change from "1" to "0". If the TQ bit does not return to "0" even after the elapse of several cycle times, the target CUnet station is either not connected to the network or is not in operation. In this case, write "0" to the TQ bit and terminate mode checking. Even if the TQ bit remains "1" continuously, although the PING instruction cannot be issued, it does not affect any other functions of the MKY43.

Table 4-2 Type Codes

Type code set at bits 8 to 12 of QCR	CUnet IC Mode	Status of frame option
00H	MEM Mode	0
01H	MEM Mode	1
02H	IO Mode	0
03H	IO Mode	1
04H	MEM mode not based on current status by owned expansion	---
05H to 1FH	Maker reserve	

Caution For "Frame option" in Table 4-2, refer to ***"4.4.9 Frame Option [for HUB]"***. For "Owned expansion", refer to ***"3.6 Setting Station Addresses and Owned Area"*** and ***"4.2.1 Details of Owned Area"***.

4.4.8 Global Memory Monitor (GMM) Function

The MKY43 has a global memory data monitoring function only for receiving packets from other CUnet stations based on cyclic time sharing without linking with other CUnet stations. This function is called "Global Memory Monitor (GMM)" and a CUnet station operated with this function is called a "GMM station".

When using the MKY43 as a GMM station, operate as follows with the user system program:

(1) Check that the START bit of the SCR (System Control Register) is "0".
(2) Write "1" to the GMM bit of the SCR.

To cancel using as a GMM station, write 0 to the GMM bit with the user system program.

In addition to monitoring described in ***"4.4.1 Monitoring before Network Start"***, the MKY43 used as a GMM station can monitor data in Global Memory (GM) that executes "memory data sharing" in other CUnet stations.

The concept of owned area is not applied to the MKY43 used as a GMM station. Therefore, the setting of Station Addresses (SAs) and (OWN widths) is all ignored.

The Receive Flag Register (RFR) in the MKY43 used as a GMM station is updated when the Station Time (ST) indicated by bits 0 to 6 of the SCR is "0" and the status of receiving packets from other CUnet stations is reflected thereafter. Therefore, when the ST exceeds the value stored in the Final Station Register (FSR) (at period of public frame), the following can be recognized by reading the RFR:

(1) If there is a bit at "1", the CUnet station with the SA corresponding to that bit is operating on a network.
(2) The latest data is in the memory block of GM corresponds to the bit at "1".

It is possible to recognize that a resized cycle is operating when the values stored in bits 0 to 5 (FS0 to FS5) of the FSR are not the initial value of 63 (3FH).

A GMM station is not included in "64", which is the maximum number of connectable CUnet ICs defined in the CUnet protocol. As many GMM stations can be connected as the network electrical performance allows.

Data of the RFR changes sequentially and very fast. When a low-speed CPU references the RFR with the aim of recognizing (1) mentioned above, freezing the RFR by ALM (ALarM) interrupt enables the CPU to reference static RFR. For details, refer to ***"4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation"***.

4.4.9 Frame Option [for HUB]

The MKY43 conforms to the frame option defined in the CUnet protocol. The frame option causes the Length Of Frame (LOF) to be “256”. This option enables insertion of a HUB (communications cable branching unit) into the CUnet network.

The CUnet where a HUB (communications cable branching unit) is inserted into a network provides high degree of flexibility in connecting network cable, resulting in expanded user systems (for details, refer to ***“HUB-IC User's Manual”***) as shown below:

(1) Cables in network can be extended
(2) Cables in network can be branched
(3) Less concern for termination resistors at each CUnet station device
(4) Star topology possible
(5) Easy support for optical fibers

4.4.9.1 Number of Insertable HUBs

In a CUnet network to which the frame option is set, up to two HUBs (communications cable branching units) can be inserted (Fig. 4.36).

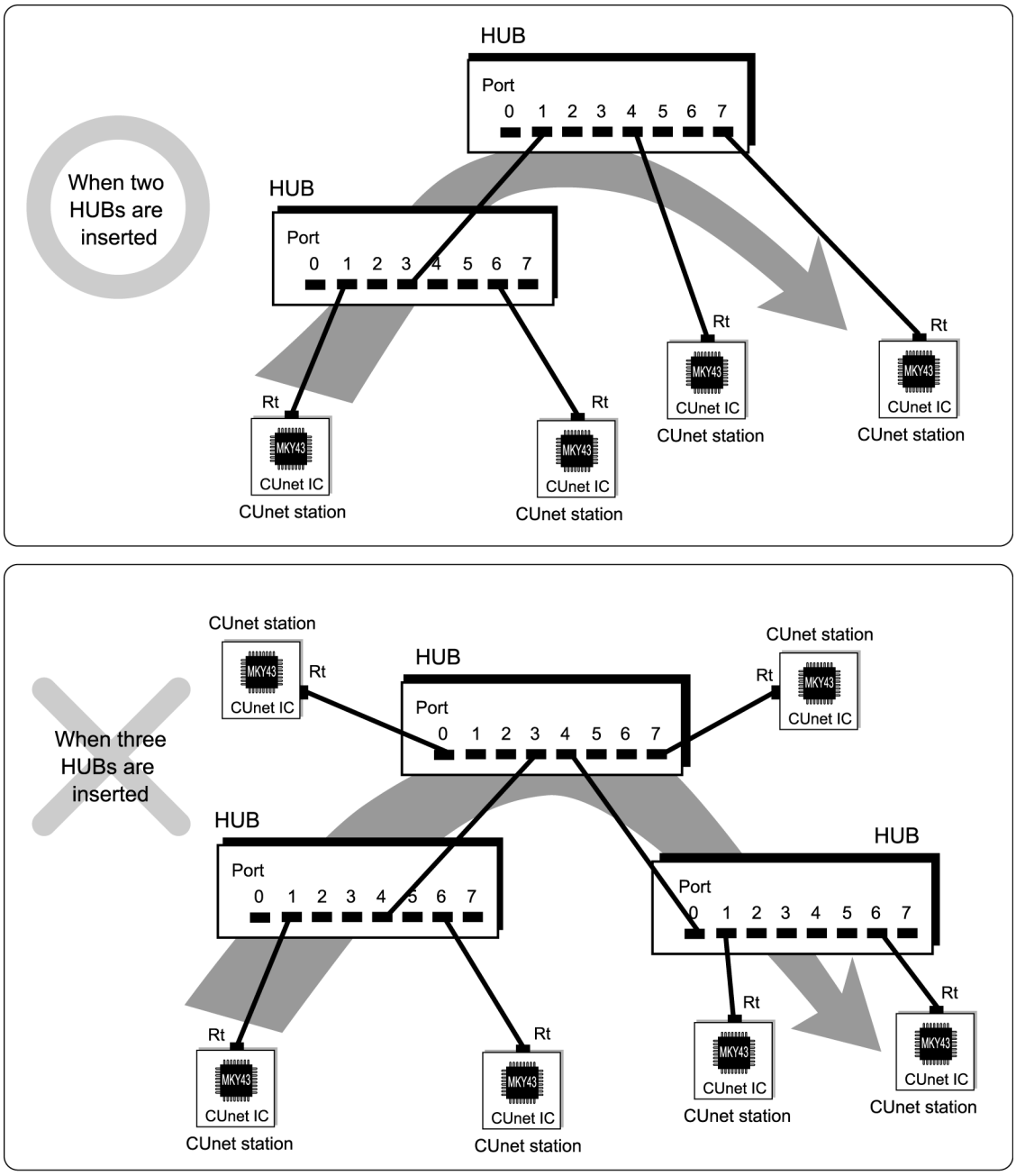


Fig. 4.36 Number of Inserted HUBs

4.4.9.2 Setting of Frame Option

To set the frame option, write “1” to bit 15 (LFS: Long Frame Select) of the Basic Control Register (BCR) in Step (2)-3 of ***“4.1.3 Initialization and Start-up of Communication”*** (Fig. 4.37).
The frame option is set to all CUnet stations in the mutual link process with other CUnet stations after network start. It is also set automatically in the CUnet station which is later connected (turned on) to the network operating with the frame option set. Therefore, by writing “1” to the LFS bit of the BCR, one (or multiple) CUnet station(s) connected to a network changes to a CUnet which operates in a cycle with a Length Of Frame (LOF) of “256”.
In the MKY43 to which the frame option is completely set, bit 14 (LF: Long Frame) of the SCR is set to “1”. To check the setting of the frame option by the user system program, read the SCR to check that bit 14 (LF) is “1”.

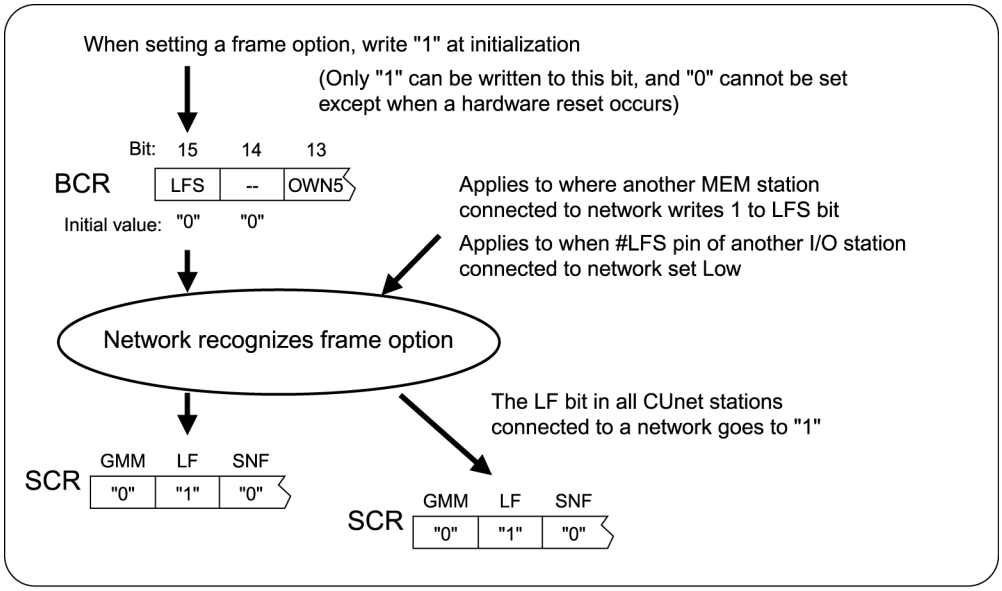

When setting a frame option, write "1" at initialization
(Only "1" can be written to this bit, and "0" cannot be set except when a hardware reset occurs)
Bit: 15 14 13
BCR
LFS
--
OWN5
Initial value: "0" "0"
Applies to where another MEM station connected to network writes 1 to LFS bit
Applies to when #LFS pin of another I/O station connected to network set Low
Network recognizes frame option
The LF bit in all CUnet stations connected to a network goes to "1"
SCR
GMM LF SNF
"0" "1" "0"
SCR
GMM LF SNF
"0" "1" "0"

Fig. 4.37 Setting of Frame Option

The CUnet that operates with the LF bit at “1” has an LOF of “256” and provides longer cycle time as compared with the case where a frame option is not used (refer to ***“4.1.6 Cycle Time of CUnet”***).

Caution The LF bit of the SCR can be cleared only by an MKY43 hardware reset. In all CUnet stations to link with the MEM stations where the LF bit is “1”, “1” is set to the LF bit. Therefore, when canceling the frame option for the system, perform an operation to activate a hardware reset for all CUnet ICs in the system.

4.5 Interrupt Trigger Generation Function

The MKY43 has two output pins (#INT0, #INT1 pin) that can supply signals to the interrupt trigger pins of a user CPU.

The two interrupt trigger output pins can be used separately as follows:

(1) #INT0 pin to output frequently-used interrupt trigger signals

(2) #INT1 pin to output interrupt trigger signals for processing error and failure that occur rarely

This section describes the operation of the interrupt trigger generation function and the operation of the MKY43 associated with the interrupt trigger output.

4.5.1 Operation of #INT0 Pin

The interrupt trigger generation function of the #INT0 pin can be used through the following operation with the user system program (Fig. 4.38):

(1) The INTerrupt 0 Control Register (INT0CR) is a register that "enables" the function of the #INT0 pin. Of the INT0CR interrupt factors, write "1" to the bit corresponding to the interrupt factor that the user system requires and "enable" the function of the #INT0 pin.

(2) When the enabled interrupt factor by the INT0CR occurs, status "1" that occurred in the INTerrupt 0 Status Register (INT0SR) with the same bit assignment as that of the INT0CR is held and a Low level is output from the #INT0 pin.

(3) The user system program can recognize which interrupt factor generated an interrupt trigger by reading the INT0SR.

(4) Write "1" to the corresponding interrupt factor bit of the INT0SR after completion of interrupt handling by the user system program. This clears the "1"-held status of INT0SR and the corresponding bit returns to "0".

(5) When all bits of the INT0SR go to "0", the #INT0 pin returns to hold its High-level output.

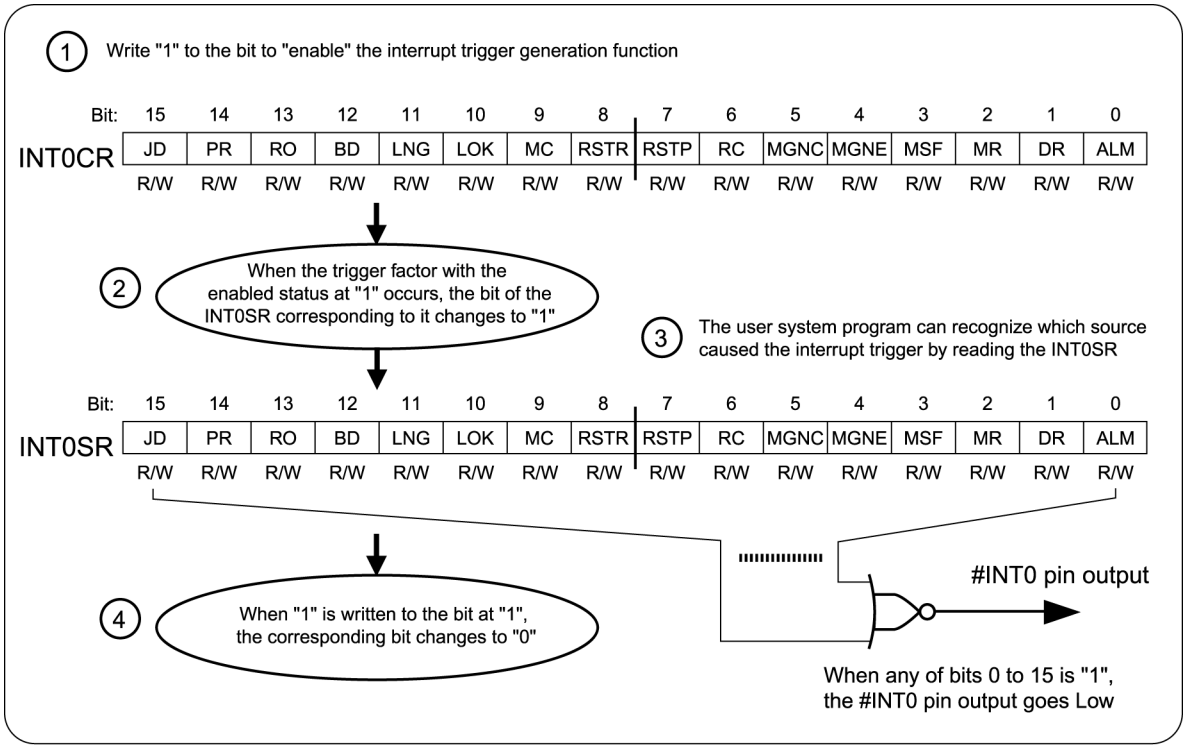

1
Write "1" to the bit to "enable" the interrupt trigger generation function
Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
INT0CR JD PR RO BD LNG LOK MC RSTR RSTP RC MGNC MGNE MSF MR DR ALM
R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W
2
When the trigger factor with the enabled status at "1" occurs, the bit of the INT0SR corresponding to it changes to "1"
3
The user system program can recognize which source caused the interrupt trigger by reading the INT0SR
Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
INT0SR JD PR RO BD LNG LOK MC RSTR RSTP RC MGNC MGNE MSF MR DR ALM
R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W
4
When "1" is written to the bit at "1", the corresponding bit changes to "0"
#INT0 pin output
When any of bits 0 to 15 is "1", the #INT0 pin output goes Low

Fig. 4.38 Interrupt Trigger Generating Function

The user system program needs to specify beforehand the interrupt generation time for the interrupt factors ALM (ALarM) and DR (Data Renewal). The lnterrupt Timing 0 Control Register (IT0CR) is used to specify the timing for the #INT0 pin (Fig. 4.39).
Write the station time to generate the interrupt factor ALM to bits 0 to 6 (ALM0 to ALM6) of the IT0CR.
Write the station time to generate the interrupt factor DR to bits 8 to 14 (DR0 to DR6) of the IT0CR.

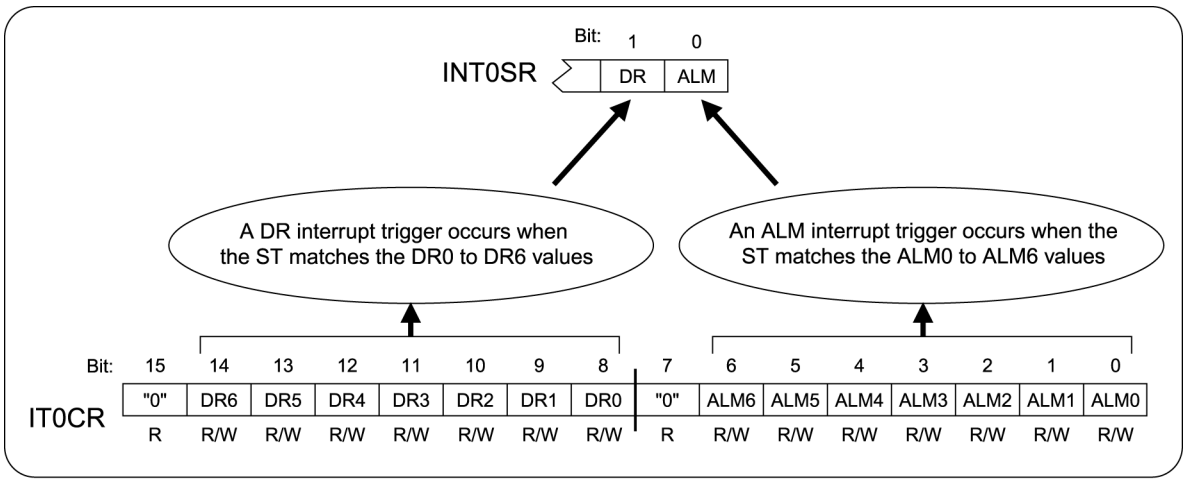

Bit: 1 0
INT0SR
DR
ALM
A DR interrupt trigger occurs when the ST matches the DR0 to DR6 values
An ALM interrupt trigger occurs when the ST matches the ALM0 to ALM6 values
Bit: 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
IT0CR
"0" DR6 DR5 DR4 DR3 DR2 DR1 DR0 "0" ALM6 ALM5 ALM4 ALM3 ALM2 ALM1 ALM0
R R/W R/W R/W R/W R/W R/W R/W R R/W R/W R/W R/W R/W R/W R/W

Fig. 4.39 DR and ALM Interrupt Trigger Generation Timing

Reference

When status is held in the INT0SR, it is not cleared even if the corresponding enable bit of the INT0CR is canceled.
After a hardware reset is activated, all the enable bits of the interrupt factor are initialized to “0” (disabled).

4.5.2 Retrigger Function

Multiple interrupt factors can be set in the #INT0 pin outputting interrupt signals. If the user system program uses an interrupt that enabled two or more interrupt factors, the pin output may change to Low again after "five clocks" right after the output returns to High. This is called a "retrigger function" (Fig. 4.40). The retrigger function is enabled when:

(1) Statuses are held in the INT0SR and some of them are cleared.
For example, "1000H" is written when data in the INT0SR is "1004H".

(2) A new enabled interrupt factor occurs concurrently with a write operation to clear the statuses held in the INT0SR. For example, a new enabled interrupt factors "0004H" occurs at the same time writing of "1000H" when data in the INT0SR is "1000H".

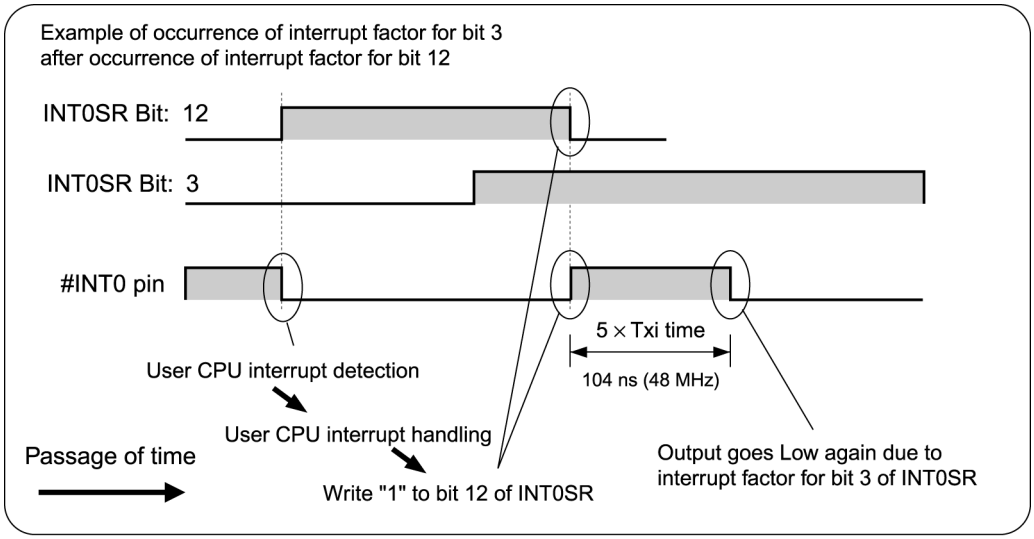

Example of occurrence of interrupt factor for bit 3
after occurrence of interrupt factor for bit 12
INT0SR Bit: 12
INT0SR Bit: 3
#INT0 pin
5 × Txi time
104 ns (48 MHz)
User CPU interrupt detection
User CPU interrupt handling
Passage of time
Write "1" to bit 12 of INT0SR
Output goes Low again due to
interrupt factor for bit 3 of INT0SR

Fig. 4.40 Operation Example of Retrigger Function

Even if the interrupt controller of a user CPU is edge-detection type, the retrigger function of the MKY43 prevents interrupts from being lost unexpectedly.
If the interrupt controller is a type that enables the next interrupt occurrence when the End Of Interrupt (EOI) code is issued from the CPU, it may be necessary to consider the order of issuing the EOI code and clearing the status of the INT0SR described in item (4) of ***"4.5.1 Operation of #INT0 Pin"***, depending on whether the interrupt controller is edge-detection type or level-detection type.

Edge detection type: The status of the INT0SR is cleared after the EOI code is issued. If the INT0SR status is cleared before issuing EOI, the retrigger function causes the status to change from High to Low with acceptance of the next interrupt disabled. This may prevent the user CPU from processing interrupts.
Level detection type: The EOI code is issued after the status of the INT0SR is cleared. If the INT0SR status is cleared after issuing EOI, the Low-level status may be detected again and interrupts may be accepted again.

Caution An algorithm of the interrupt handling and canceling procedure depend on the user system, such as the type of the user CPU and peripheral hardware. Use the MKY43 appropriately according to the user system.

4.5.3 Interrupt Factors

The INTerrupt 0 Control Register (INT0CR) has the following 16 types of interrupt factors that can be enabled (Table 4-3).

Table 4-3 Interrupt Factors

Interrupt factor	Bit	When trigger output occurs (requirements)	Reference
ALM: ALarM	0	When ST during cycle reaches time previously specified to IT0CR This interrupt trigger occurs every cycle.	4.1.7 Detailed Timing during Cycle
DR: Data Renewal	1	Only when data transition of GM corresponding to detection bit previously set to DRCR detected and when ST during cycle reaches time previously specified to IT0CR	4.2.4 Detection of Global Memory Data Transition
MR: Mail Receive	2	When mail received from other CUnet stations	4.3.2 Operation for Mail Reception
MSF: Mail Send Finish	3	When mail sending to other CUnet stations terminates (correctly or incorrectly)	4.3.3 Operation for Mail Sending and after Completion of Sending
MGNE: Member Group Not Equal	4	When bit 4 (MGNE) of SSR changes from “0” to “1”	4.2.3.6 Member Group Register (MGR)
MGNC: Member Group Not Collect	5	When bit 5 (MGNC) of SSR changes from “0” to “1”	4.2.3.6 Member Group Register (MGR)
RC: Resize Complete	6	When resizing of self-station completed in response to resize command from another CUnet station	4.4.2.1 Resizing
RSTP: Run SToP	7	When network stops	4.1.8 Network Stop
RSTR: Run STaRt	8	When MKY43 enters RUN phase	4.1.3 Initialization and Start-up of Communication
MC: Member Change	9	When number of “1s” of member flag bit increases or decreases	4.2.3.7 Detection of Member Increase and Decrease
LOK: Link group OK	10	When “Link OK” judged by checking LFR bit corresponding to LGR with bit = “1”	4.2.3.3 Link Group Register (LGR)
LNG: Link group No Good	11	When “Link NG” (No Good) judged by checking LFR bit corresponding to LGR with bit = “1”	4.2.3.3 Link Group Register (LGR)
BD: Break Detect	12	When CUnet station in BREAK phase detected	4.4.3 Detection and Handling of CUnet Station in BREAK Phase
RO: Resize Overlap	13	When resize overlap occurs	4.4.2.3 Resize Overlap (RO)
PR: Ping Receive	14	When PING instruction received from another CUnet station	4.4.6 PING Instruction
JD: Jammer Detect	15	When jammer detected	4.4.4 Detection and Handling of Jammer

4.5.4 Operation of #INT1 Pin

The operation of the #INT1 pin is the same as that of the #INT0 pin described in ***"4.5.1 Operation of #INT0 Pin"*** to ***"4.5.3 Interrupt Factors"***.
The register to "enable" the function of the #INT1 pin is INTerrupt 1 Control Register (INT1CR).
The register to hold the status of the #INT1 pin is INTerrupt 1 Status Register (INT1SR).
The #INT1 pin also has a retrigger function.
The register to specify the timing of the interrupt factors "ALarM (ALM)" and "Data Renewal (DR)" for the #INT1 pin is Interrupt Timing 1 Control Register (IT1CR).

4.5.5 Precautions for Specifying Timing of Interrupt Trigger Generation

The values to set timing to the IT0CR and IT1CR are "0 to 127 (00H to 7FH)" but a CUnet cycle uses the values stored in the Final Station Register (FSR) with up to "2" added. When numerical values exceeding these values are written to the IT0CR or IT1CR, corresponding interrupt triggers are not generated. Do not write an incorrect value.
In particular, the DR generation timing is the update timing of the DRFR described in ***"4.2.4.3 Transition Timing of DR Flag Bit and DRFR Bits from "1" to "0""***. Therefore, if numerical values exceeding the values stored in the Final Station Register (FSR) with "2" added are written, the DRFR is not updated.

4.5.6 Precautions for Use of Data Renewal (DR) Interrupt Trigger

Both pins of the #INT0 and #INT1 cannot be used at the same time for Data Renewal (DR) which is the interrupt factor. Use either one.
When the INT0CR is first "enabled", writing "1" to the enable bit of the INT1CR is protected. To the contrary, when the INT1CR is first "enabled", writing "1" to the enable bit of the INT0CR is protected.

Interrupt trigger generation timing of the DR is the time set at bits 8 to 14 of the IT0CR when the INT0CR is enabled and the time set at bits 8 to 14 of the IT1CR when the INT1CR is enabled.
The same is true for the timing of bit 11 (DR: Data Renewal) of the System Status Register (SSR) and the Data Renewal Flag Register (DRFR) bits described in ***"4.2.4.3 Transition Timing of DR Flag Bit and DRFR Bits from "1" to "0""***. (The time set at bits 8 to 14 of the IT0CR when the INT0CR is enabled and the time set at bits 8 to 14 of the IT1CR when the INT1CR is enabled). However, when DRs of the INT0CR and INT1CR are disabled, the timing of bit 11 of the SSR and DRFR bits changing from "1" to "0" is the time set at bits 8 to 14 of the IT0CR.

4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation

The MKY43 freezes specific registers while outputting specific interrupt triggers.
Freezing registers prevents specific registers related to interrupt factors from being updated after interrupt triggers are output from the MKY43 (and before processing is referenced by the interrupt handling program of the user system). Frozen registers are duplicated within the MKY43 and only the part that can be read from the user system is frozen. Therefore, when the status of specific interrupt triggers is cleared at completion of processing by the interrupt handling program of the user system, the registers are immediately unfrozen and return their current status.
Table 4-4 lists the correspondence between frozen registers and interrupt factors.

Table 4-4 Frozen Registers

Interrupt factor	Frozen register and flag bit
ALM (ALarM) MC (Member Change) LOK (Link group OK) LNG (Link group No Good)	All bits of RFR All bits of LFR Bit 12 (LOK) of SSR
DR (Data Renewal)	All bits of DRFR Bit 11 (DR) of SSR

If the Member Change (MC) interrupt occurs, the Member Flag Register (MFR) is not frozen. The MFR is updated at “the starting point of status management”, so the processing started by the MC interrupt should be cared so as not to refer to the MFR, going over the next “starting point of status management”.

4.5.8 BD/RO/JD Interrupt Generation

For Break Detect (BD) interrupt, the interrupt whose factor has occurred while the detect flag of the SSR is “1” is not generated even if the target interrupt factor bit is set to “1”. Therefore, at the BD interrupt setting, also set last the detect flag of the SSR to “0”.
This applies to the Resize Overlap (RO) interrupt and Jammer Detect (JD) interrupt similarly.

Chapter 5 Register Reference

This chapter provides references for registers of the MKY43 in the address order.

Chapter 5 Register Reference

This chapter provides references for registers of the MKY43 in the address order (Table 5-1).

The description in this chapter conforms to the following format:

(1) Register addresses are represented by starting addresses of 16-bit access.
(2) Data bits are represented by 16-bit access.

When referencing this chapter, consider the following points:

(1) The MKY43 has a 16-bit wide register and a 64-bit wide register.
(2) Register addresses differ depending on the data bus width, access width (such as 8-bit access in 16-bit wide data bus), and endian type of CPU connected to the MKY43. 8-bit access not mentioned in this chapter requires address conversion before use.

Table 5-1 Register List

Section	Address value	Area name	Register name	Bit count	Target function	Page
5.1	300H to 307H	RFR	Receive Flag Register	64	Link detection	5-5
5.2	308H to 30FH	LFR	Link Flag Register	64		5-6
5.3	310H to 317H	MFR	Member Flag Register	64	Member detection	5-7
5.4	318H to 31FH	DRFR	Data Renewal Flag Register	64	Data transition detection	5-8
5.5	320H to 327H	LGR	Link Group Register	64	Link detection	5-9
5.6	328H to 32FH	MGR	Member Group Register	64	Member detection	5-10
5.7	330H to 337H	DRCR	Data Renewal Check Register	64	Data transition detection	5-11
5.8	338H	RHCR0	Read Hazard Control Register 0	16	Read hazard protection	5-12
5.9	33AH	RHCR1	Read Hazard Control Register 1	16		5-12
5.10	33CH	WHCR0	Write Hazard Control Register 0	16	Write hazard protection	5-13
5.11	33EH	WHCR1	Write Hazard Control Register 1	16		5-13
5.12	340H	MSLR	Mail Send Limit time Register	16	Mail sending	5-14
5.13	342H	MSRR	Mail Send Result Register	16		5-14
5.14	344H	MESR	Mail Error Status Register	16		5-15
5.15	346H	MSCR	Mail Send Control Register	16		5-16
5.16	348H	MR0CR	Mail Receive 0 Control Register	16	Mail reception	5-17
5.17	34AH	MR1CR	Mail Receive 1 Control Register	16		5-18
5.18	34CH	CCTR	Care CounTer Register	16	System support	5-19
5.19	34EH	UTCR	UTility pin Control Register	16		5-20
5.20	350H	QCR	Query Control Register	16		5-21
5.21	352H	NFSR	New Final Station Register	16	System	5-22
5.22	354H	FSR	Final Station Register	16		5-22
5.23	356H	BCR	Basic Control Register	16		5-23
5.24	358H	INT0CR	INTerrupt 0 Control Register	16	Interrupt control	5-24
5.25	35AH	INT1CR	INTerrupt 1 Control Register	16		5-26
5.26	35CH	IT0CR	Interrupt Timing 0 Control Register	16		5-27
5.27	35EH	IT1CR	Interrupt Timing 1 Control Register	16		5-27
5.28	360H	INT0SR	INTerrupt 0 Status Register	16		5-28
5.29	362H	INT1SR	INTerrupt 1 Status Register	16		5-30
5.30	364H	SSR	System Status Register	16	System	5-32
5.31	366H	SCR	System Control Register	16		5-34
5.32	368H to 36FH	CCR	Chip Code Register	64		5-36
5.33	370H to 377H	RHPB0	Read Hazard Protection Buffer 0	64	Read hazard protection	5-37
5.34	378H to 37FH	RHPB1	Read Hazard Protection Buffer 1	64		5-38
5.35	380H to 387H	WHPB0	Write Hazard Protection Buffer 0	64	Write hazard protection	5-39
5.36	388H to 38FH	WHPB1	Write Hazard Protection Buffer 1	64		5-40

5.1 Receive Flag Register (RFR)

Address: 300H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFR 15	RFR 14	RFR 13	RFR 12	RFR 11	RFR 10	RFR 9	RFR 8	RFR 7	RFR 6	RFR 5	RFR 4	RFR 3	RFR 2	RFR 1	RFR 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 302H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFR 31	RFR 30	RFR 29	RFR 28	RFR 27	RFR 26	RFR 25	RFR 24	RFR 23	RFR 22	RFR 21	RFR 20	RFR 19	RFR 18	RFR 17	RFR 16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 304H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFR 47	RFR 46	RFR 45	RFR 44	RFR 43	RFR 42	RFR 41	RFR 40	RFR 39	RFR 38	RFR 37	RFR 36	RFR 35	RFR 34	RFR 33	RFR 32
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 306H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFR 63	RFR 62	RFR 61	RFR 60	RFR 59	RFR 58	RFR 57	RFR 56	RFR 55	RFR 54	RFR 53	RFR 52	RFR 51	RFR 50	RFR 49	RFR 48
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[Functional description]

This register stores the individual receiving status that guarantees data in individual memory blocks (MBs) constituting Global Memory (GM) is written by the latest cycle when the START bit (bit 8) of the SCR is set to "1". Bit 0 corresponds to MB0, bit 1 to MB1, and bit 63 to MB63.

The bit corresponding to the self-station owned area of this register changes to "1" when the START bit of the SCR is set to "1"; the bit corresponding to the self-station owned area of this register changes to "0" when the START bit of the SCR is set to "0".

For details of the bit transition timing of this register, refer to ***"4.2.3 Quality Assurance of GM Data"***.

The bit status of this register freezes during the output of ALM (ALarM), MC (Member Change), LOK (Link group OK), and LNG (Link group No Good) interrupt triggers. For details, refer to ***"4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation"***.

5.2 Link Flag Register (LFR)

Address: 308H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LFR 15	LFR 14	LFR 13	LFR 12	LFR 11	LFR 10	LFR 9	LFR 8	LFR 7	LFR 6	LFR 5	LFR 4	LFR 3	LFR 2	LFR 1	LFR 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 30AH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LFR 31	LFR 30	LFR 29	LFR 28	LFR 27	LFR 26	LFR 25	LFR 24	LFR 23	LFR 22	LFR 21	LFR 20	LFR 19	LFR 18	LFR 17	LFR 16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 30CH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LFR 47	LFR 46	LFR 45	LFR 44	LFR 43	LFR 42	LFR 41	LFR 40	LFR 39	LFR 38	LFR 37	LFR 36	LFR 35	LFR 34	LFR 33	LFR 32
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 30EH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LFR 63	LFR 62	LFR 61	LFR 60	LFR 59	LFR 58	LFR 57	LFR 56	LFR 55	LFR 54	LFR 53	LFR 52	LFR 51	LFR 50	LFR 49	LFR 48
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[Functional description]

This register stores the individual flags that guarantees data in individual memory blocks (MBs) constituting Global Memory (GM) are written by the latest cycle and data in MBs of a self-station is copied to each CUnet station. Bit 0 corresponds to the station address (SA) 0 and MB0, bit 1 to SA1 and MB1, and bit 63 to SA63 and MB63.

The bit corresponding to the self-station owned area of this register changes to "1" when the START bit of the SCR is set to "1"; the bit corresponding to the self-station owned area of this register changes to "0" when the START bit of the SCR is set to "0".

For details of the bit transition timing of this register, refer to ***"4.2.3 Quality Assurance of GM Data"***.

The bit status of this register freezes during the output of ALM (ALarM), MC (Member Change), LOK (Link group OK), and LNG (Link group No Good) interrupt triggers. For details, refer to ***"4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation"***.

5.3 Member Flag Register (MFR)

Address: 310H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MFR 15	MFR 14	MFR 13	MFR 12	MFR 11	MFR 10	MFR 9	MFR 8	MFR 7	MFR 6	MFR 5	MFR 4	MFR 3	MFR 2	MFR 1	MFR 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 312H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MFR 31	MFR 30	MFR 29	MFR 28	MFR 27	MFR 26	MFR 25	MFR 24	MFR 23	MFR 22	MFR 21	MFR 20	MFR 19	MFR 18	MFR 17	MFR 16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 314H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MFR 47	MFR 46	MFR 45	MFR 44	MFR 43	MFR 42	MFR 41	MFR 40	MFR 39	MFR 38	MFR 37	MFR 36	MFR 35	MFR 34	MFR 33	MFR 32
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 316H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MFR 63	MFR 62	MFR 61	MFR 60	MFR 59	MFR 58	MFR 57	MFR 56	MFR 55	MFR 54	MFR 53	MFR 52	MFR 51	MFR 50	MFR 49	MFR 48
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[Functional description]

This register stores the individual member status in which “1” is set when “Link Established” is recognized consecutively three times, and “0” is set when “Link unestablished” is recognized consecutively three times. Bit 0 corresponds to the station address (SA) 0, bit 1 to SA1, and bit 63 to SA63. The bit of this register is updated at the lead point of Station Time (ST) matching the SA of a self-station (at the starting point of status management).

All the bits of this register keep “0” when the START bit of the SCR (System Control Register) is “0” and the GMM bit of the SCR is “1”.

5.4 Data Renewal Flag Register (DRFR)

Address: 318H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRFR 15	DRFR 14	DRFR 13	DRFR 12	DRFR 11	DRFR 10	DRFR 9	DRFR 8	DRFR 7	DRFR 6	DRFR 5	DRFR 4	DRFR 3	DRFR 2	DRFR 1	DRFR 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 31AH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRFR 31	DRFR 30	DRFR 29	DRFR 28	DRFR 27	DRFR 26	DRFR 25	DRFR 24	DRFR 23	DRFR 22	DRFR 21	DRFR 20	DRFR 19	DRFR 18	DRFR 17	DRFR 16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 31CH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRFR 47	DRFR 46	DRFR 45	DRFR 44	DRFR 43	DRFR 42	DRFR 41	DRFR 40	DRFR 39	DRFR 38	DRFR 37	DRFR 36	DRFR 35	DRFR 34	DRFR 33	DRFR 32
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 31EH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRFR 63	DRFR 62	DRFR 61	DRFR 60	DRFR 59	DRFR 58	DRFR 57	DRFR 56	DRFR 55	DRFR 54	DRFR 53	DRFR 52	DRFR 51	DRFR 50	DRFR 49	DRFR 48
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[Functional description]

This register indicates the result of detection of data transition for a Memory Block (MB) set to the DRCR (Data Renewal Check Register). Bit 0 of the DRFR corresponds to MB0, bit 1 to MB1, and bit 63 to MB63. The bit corresponding to the MB where data transition is detected keeps "1". For details of the timing of bit transition of this register, refer to ***"4.2.4 Detection of Global Memory Data Transition"***.

The bit status of this register freezes during the output of the DR (Data Renewal) interrupt trigger. For details of freezing, refer to ***"4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation"***.

The function of this register is also enabled when the MKY43 operates as a GMM (Global Memory Monitor) station.

5.5 Link Group Register (LGR)

Address: 320H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LGR 15	LGR 14	LGR 13	LGR 12	LGR 11	LGR 10	LGR 9	LGR 8	LGR 7	LGR 6	LGR 5	LGR 4	LGR 3	LGR 2	LGR 1	LGR 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 322H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LGR 31	LGR 30	LGR 29	LGR 28	LGR 27	LGR 26	LGR 25	LGR 24	LGR 23	LGR 22	LGR 21	LGR 20	LGR 19	LGR 18	LGR 17	LGR 16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 324H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LGR 47	LGR 46	LGR 45	LGR 44	LGR 43	LGR 42	LGR 41	LGR 40	LGR 39	LGR 38	LGR 37	LGR 36	LGR 35	LGR 34	LGR 33	LGR 32
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 326H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LGR 63	LGR 62	LGR 61	LGR 60	LGR 59	LGR 58	LGR 57	LGR 56	LGR 55	LGR 54	LGR 53	LGR 52	LGR 51	LGR 50	LGR 49	LGR 48
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register sets the bit for monitoring the LFR (Link Flag Register) status. The bits of this register correspond to the bits of the LFR.

When the bits of this register are set to “1” to set the CUnet station whose link status is monitored, the link status of any CUnet station can be monitored collectively.

5.6 Member Group Register (MGR)

Address: 328H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MGR 15	MGR 14	MGR 13	MGR 12	MGR 11	MGR 10	MGR 9	MGR 8	MGR 7	MGR 6	MGR 5	MGR 4	MGR 3	MGR 2	MGR 1	MGR 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 32AH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MGR 31	MGR 30	MGR 29	MGR 28	MGR 27	MGR 26	MGR 25	MGR 24	MGR 23	MGR 22	MGR 21	MGR 20	MGR 19	MGR 18	MGR 17	MGR 16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 32CH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MGR 47	MGR 46	MGR 45	MGR 44	MGR 43	MGR 42	MGR 41	MGR 40	MGR 39	MGR 38	MGR 37	MGR 36	MGR 35	MGR 34	MGR 33	MGR 32
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 32EH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MGR 63	MGR 62	MGR 61	MGR 60	MGR 59	MGR 58	MGR 57	MGR 56	MGR 55	MGR 54	MGR 53	MGR 52	MGR 51	MGR 50	MGR 49	MGR 48
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register sets the bit for monitoring the MFR (Member Flag Register) status. The bits of this register correspond to the bits of the MFR.

When the bits of this register are set to "1" to set a member group, the member status of any CUnet station can be monitored collectively.

5.7 Data Renewal Check Register (DRCR)

Address: 330H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRCR 15	DRCR 14	DRCR 13	DRCR 12	DRCR 11	DRCR 10	DRCR 9	DRCR 8	DRCR 7	DRCR 6	DRCR 5	DRCR 4	DRCR 3	DRCR 2	DRCR 1	DRCR 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 332H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRCR 31	DRCR 30	DRCR 29	DRCR 28	DRCR 27	DRCR 26	DRCR 25	DRCR 24	DRCR 23	DRCR 22	DRCR 21	DRCR 20	DRCR 19	DRCR 18	DRCR 17	DRCR 16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 334H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRCR 47	DRCR 46	DRCR 45	DRCR 44	DRCR 43	DRCR 42	DRCR 41	DRCR 40	DRCR 39	DRCR 38	DRCR 37	DRCR 36	DRCR 35	DRCR 34	DRCR 33	DRCR 32
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 336H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRCR 63	DRCR 62	DRCR 61	DRCR 60	DRCR 59	DRCR 58	DRCR 57	DRCR 56	DRCR 55	DRCR 54	DRCR 53	DRCR 52	DRCR 51	DRCR 50	DRCR 49	DRCR 48
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register presets the bit corresponding to a Memory Block (MB) where data transition is detected when using the function to detect data transition of Global Memory (GM). The bit where "1" is written is to be detected. Bit 0 of the DRCR corresponds to MB0, bit 7 to MB7, and bit 63 to MB63.
The function of this register is also enabled when the MKY43 operates as a GMM (Global Memory Monitor) station.

Caution The function to detect data transition does not operate for the memory block owned by the self-station, even if the target DRCR has been set to "1".

5.8 Read Hazard Control Register 0 (RHCR0)

Address: 338H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	---	---	---	---	---	MB5	MB4	MB3	MB2	MB1	MB0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register controls the read hazard protection function.

Write the Memory Block (MB; "00H to 3FH") address of the copy source to this register in order to copy the 64-bit data in Memory Block (MB) form Global Memory (GM) to the RHPB0 (Read Hazard Protection Buffer 0).

5.9 Read Hazard Control Register 1 (RHCR1)

Address: 33AH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	---	---	---	---	---	MB5	MB4	MB3	MB2	MB1	MB0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register controls the read hazard protection function.

Write the Memory Block (MB; "00H to 3FH") address of the copy source to this register in order to copy the 64-bit data in Memory Block (MB) form Global Memory (GM) to the RHPB1 (Read Hazard Protection Buffer 1).

5.10 Write Hazard Control Register 0 (WHCR0)

Address: 33CH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	---	---	---	---	---	MB5	MB4	MB3	MB2	MB1	MB0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register controls the write hazard protection function.

Write the Memory Block (MB; "00H to 3FH") address of the write destination to this register in order to write the 64-bit data in the WHPB0 (Write Hazard Protection Buffer 0) collectively to the specified Memory Block (MB) in the Global Memory (GM).

5.11 Write Hazard Control Register 1 (WHCR1)

Address: 33EH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	---	---	---	---	---	MB5	MB4	MB3	MB2	MB1	MB0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register controls the write hazard protection function.

Write the Memory Block (MB; "00H to 3FH") address of the write destination to this register in order to write the 64-bit data in the WHPB1 (Write Hazard Protection Buffer 1) collectively to the specified Memory Block (MB) in the Global Memory (GM).

Caution In the following cases, the Global Memory (GM) is write-protected.
Similarly, the WHCR0 and WHCR1 are also write-protected.

- When the GMM bit of the System Control Register (SCR) is "1"
- When the START bit of the SCR is "1" and any MB value other than that in the owned area is written to the WHCR0 or the WHCR1

5.12 Mail Send Limit time Register (MSLR)

Address: 340H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	LMT 12	LMT 11	LMT 10	LMT 9	LMT 8	LMT 7	LMT 6	LMT 5	LMT 4	LMT 3	LMT 2	LMT 1	LMT 0
Initial value:	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register sets the time-out value of mail sending.

Write the time-out value (hexadecimal; "0004H to 1FFFH") using cycle time as one unit that is defined by the user system to the LMT0 to LMT12 (LiMit Time) bits of this register.

When bit 14 (SEND) of MSCR (Mail Send Control Register) is "1" (mail sending is on), this register is write-protected.

When a hardware reset is activated, 1FFFH is set as the initial value in this register.

If mail sending is started while the value of this register is between "0000H to 0003H", LMFLT (LiMit time FauLT) error occurs, and the mail is not send.

5.13 Mail Send Result Register (MSRR)

Address: 342H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	RLT 12	RLT 11	RLT 10	RLT 9	RLT 8	RLT 7	RLT 6	RLT 5	RLT 4	RLT 3	RLT 2	RLT 1	RLT 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[Functional description]

This register stores the time required for mail sending.

At completion of mail sending, the cycle count (hexadecimal) that is the time required from when mail sending starts until it ends is set to the RLT0 to RLT12 (ResuLt Time) bits.

The register values are kept until the next mail sending is completed.

5.14 Mail Error Status Register (MESR)

Address: 344H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	---	---	---	---	---	STOP	LMFLT	SZFLT	TOUT	NOEX	NORDY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register indicates the status of a mail sending error that occurred after starting. The bit corresponding to the mail sending error type changes to "1".

When any data is written to addresses with bits 0 to 5, all bits are cleared to "0".

● **Bit description**

destination NOt ReaDY (NORDY) bit (bit 0)

[Function] This bit indicates that a mail sending error occurred because a destination receive buffer is not ready for reception.

destination NOt EXist (NOEX) bit (bit 1)

[Function] This bit indicates that a mail sending error occurred because the destination CUnet station set in the MSCR (Mail Send Control Register) does not exist.

limit Time OUT (TOUT) bit (bit 2)

[Function] This bit indicates that a mail sending error occurred because mail sending is completed even after the cycle count set in the MSLR (Mail Send Limit time Register) is reached.

SiZe FauLT (SZFLT) bit (bit 3)

[Function] This bit indicates that a mail sending error occurred because the set mail sending size set in the MSCR (Mail Send Control Register) is invalid.

LiMit time FauLT (LMFLT) bit (bit 4)

[Function] This bit indicates that a mail sending error occurred because the value set in the MSLR (Mail Send Limit time Register) is invalid.

communication STOPped (STOP) bit (bit 5)

[Function] This bit indicates that a mail sending error occurred because the network stopped during mail sending.

5.15 Mail Send Control Register (MSCR)

Address: 346H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR	SEND	DST5	DST4	DST3	DST2	DST1	DST0	---	---	SZ5	SZ4	SZ3	SZ2	SZ1	SZ0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register controls mail transmission for data sets written to the MSB (Mail Send Buffer).

● **Bit description**

send SiZe (SZ0 to SZ5) bit (bits 0 to 5)

[Function] These are bits where the size of datasets for mail sending is set.
Write the size (hexadecimal) of datasets for mail sending before or at the same time "1" is written to the SEND bit (bit 14). The dataset size uses 8 bytes as one unit. For example, if a dataset is 34 bytes, its size is "05H". If a dataset is a maximum of 256 bytes, its size is "20H". If "00H" or "21H to 3FH" are accidentally set as the size value, SZFLT (SiZe FauLT) error occurs, and the mail is not send.

DeSTination station address (DST0 to DST5) bit (bits 8 to 13)

[Function] These are bits where destination station addresses to which mail is sent are set.
Write the destination station address (hexadecimal) before or at the same time "1" is written to the SEND bit (bit 14).

mail SEND (SEND) bit (bit 14)

[Function] This bit starts mail transmission.
Write "1" to this bit when starting mail sending.
When the ERR bit (bit 15) is "1", this bit is write-protected.
When mail sending is terminated (correctly or stopped by an error), this bit is cleared to "0".
When this bit is "1" (mail sending is on), writing to the MSB is protected. If the MSB is read when this bit is "1", the read data is "00H".

mail send ERRor (ERR) bit (bit 15)

[Function] This bit indicates that mail sending is terminated with an error.
When an error occurs during mail sending, this bit transits to "1".
When all bits of the MESR (Mail Error Status Register) are cleared to "0", this bit is also cleared to "0".

5.16 Mail Receive 0 Control Register (MR0CR)

Address: 348H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	SRC5	SRC4	SRC3	SRC2	SRC1	SRC0	RCV	RDY	SZ5	SZ4	SZ3	SZ2	SZ1	SZ0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R

[Functional description]

This register controls the mail reception corresponding to the MRB0 (Mail Receive Buffer 0).

● **Bit description**

receive SiZe (SZ0 to SZ5) bit (bits 0 to 5)

[Function] These are bits where the dataset size (hexadecimal) of the received mail is set when the MRB0 receives mail. The dataset size uses 8 bytes as one unit.

These bits are cleared to "00H" if data is written to the RCV bit or RDY bit.

receive ReaDY (RDY) bit (bit 6)

[Function] This bit sets permission for the MRB0 to receive mail.

This bit can be operated when the START bit of the SCR is "1".

When "1" is written to this bit, the MRB0 is permitted to receive mail.

When this bit is "0", the MRB0 is inhibited from receiving mail.

This bit value cannot be set from "1" to "0" during mail reception by the MRB0. Therefore, when "0" is written, read this bit to check its status.

When "1" is written to this bit, the RCV bit is forcibly set to "0".

When this bit is "1", writing to the MRB0 is protected. If the MRB0 is read when this bit is "1", the read data is "00H".

If the START bit of the SCR changes to "0" when this bit is "1", this bit also changes to "0".

ReCeiVed (RCV) bit (bit 7)

[Function] This bit indicates the completion of mail reception.

This bit changes to "1" at completion of mail reception. The RDY bit (bit 6) changes to "0" when this bit goes to "1". When "1" is written to the RDY bit, this bit is set to "0". This bit can be forcibly set to "0" by writing "0" directly to it instead of writing "1" to the RDY bit.

When this bit is "1", writing to the MRB0 is protected.

SouRCe station address (SRC0 to SRC5) bit (bits 8 to 13)

[Function] The source station addresses (hexadecimal) are set to these bits when dataset is stored in the MRB0.

These bits are cleared to "00H" if data is written to the RCV bit or RDY bit.

5.17 Mail Receive 1 Control Register (MR1CR)

Address: 34AH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	SRC5	SRC4	SRC3	SRC2	SRC1	SRC0	RCV	RDY	SZ5	SZ4	SZ3	SZ2	SZ1	SZ0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R

[Functional description]

This register controls the mail reception corresponding to the MRB1 (Mail Receive Buffer 1).

● **Bit description**

receive SiZe (SZ0 to SZ5) bit (bits 0 to 5)

[Function] These are bits where the dataset size (hexadecimal) of the received mail is set when the MRB1 receives mail. The dataset size uses 8 bytes as one unit.
These bits are cleared to "00H" if data is written to the RCV bit or RDY bit.

receive ReaDY (RDY) bit (bit 6)

[Function] This bit sets permission for the MRB1 to receive mail.
This bit can be operated when the START bit of the SCR is "1".
When "1" is written to this bit, the MRB1 is permitted to receive mail.
When this bit is "0", the MRB1 is inhibited from receiving mail.
This bit value cannot be set from "1" to "0" during mail reception by the MRB1. Therefore, when "0" is written, read this bit to check its status.
When "1" is written to this bit, the RCV bit is forcibly set to "0".
When this bit is "1", writing to the MRB1 is protected. If the MRB1 is read when this bit is "1", the read data is "00H".
If the START bit of the SCR changes to "0" when this bit is "1", this bit also changes to "0".

ReCeiVed (RCV) bit (bit 7)

[Function] This bit indicates the completion of mail reception.
This bit changes to "1" at completion of mail reception. The RDY bit (bit 6) changes to "0" when this bit goes to "1". When "1" is written to the RDY bit, this bit is set to "0". This bit can be forcibly set to "0" by writing "0" directly to it instead of writing "1" to the RDY bit.
When this bit is "1", writing to the MRB1 is protected.

SouRCe station address (SRC0 to SRC5) bit (bits 8 to 13)

[Function] The source station addresses (hexadecimal) are set to these bits when dataset is stored in the MRB1.
These bits are cleared to "00H" if data is written to the RCV bit or RDY bit.

5.18 Care CounTer Register (CCTR)

Address: 34CH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MCC 7	MCC 6	MCC 5	MCC 4	MCC 3	MCC 2	MCC 1	MCC 0	LCC 7	LCC 6	LCC 5	LCC 4	LCC 3	LCC 2	LCC 1	LCC 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

[Functional description]

This register stores the occurrence count of LCARE and MCARE signals.

● **Bit description**

Link Care Counter (LCC0 to LCC7) bit (bits 0 to 7)

[Function] The occurrence count of the LCARE signal is stored in these bits.
The occurrence count (hexadecimal) is counted by these bits.
When the occurrence count is counted up to "FFH", the "FFH" value is kept.
The count values of these bits can be cleared to "00H" by writing "1" to the LCC0 bit (bit 0).

Member Care Counter (MCC0 to MCC7) bit (bits 8 to15)

[Function] The occurrence count of the MCARE signal is stored in these bits.
The occurrence count (hexadecimal) is counted by these bits.
When the occurrence count is counted up to "FFH", the "FFH" value is kept.
The count values of these bits can be cleared to "00H" by writing "1" to the MCC0 bit (bit 8).

5.19 UTility pin Control Register (UTCR)

Address: 34EH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	---	OE2	SS2	---	---	---	---	---	---	OE1	SS1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

[Functional description]

This register performs the setting of the UTY1 (UTilitY1) pin (pin 51) and the UTY2 (UTilitY2) pin (pin 54). The setting overview is shown in Table 5-2 below.

The UTY1 pin is controlled with the SS1 (Signal Select for utility-1) bit (bit 0) and the OE1 (Output Enable for utility-1) bit (bit 1).

The UTY2 pin is controlled with the SS2 (Signal Select for utility-2) bit (bit 8) and the OE2 (Output Enable for utility-2) bit (bit 9).

Table 5-2 Bit Definition for UTCR

UTY1 pin control

Bit 1	Bit 0	Description
OE1	SS1	
0	0	The UTY1 pin is in the high impedance state (pulled up internally).
	1	
1	0	The #PING signal is output to the UTY1 pin.
	1	The #CYCT signal is output to the UTY1 pin.

UTY2 pin control

Bit 9	Bit 8	Description
OE2	SS2	
0	0	The UTY2 pin is in the high impedance state (pulled up internally).
	1	
1	0	The #PING signal is output to the UTY2 pin.
	1	The #CYCT signal is output to the UTY2 pin.

5.20 Query Control Register (QCR)

Address: 350H

Bit;	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	TYP4	TYP3	TYP2	TYP1	TYP0	PING	TQ	TS5	TS4	TS3	TS2	TS1	TS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register controls the PING function and the function (query), which detects other CUnet station modes.

● **Bit description**

Target Station (TS0 to TS5) bit (bits 0 to 5)

[Function] These bits set the station addresses of PING and query.

Try Query (TQ) bit (bit 6)

[Function] This bit performs querying.

When "1" is written to this bit, queries are made for CUnet stations at the station addresses set to the TS0 to TS5 bits. This bit is reset to "0" after completion of querying. If there is no target CUnet station, this bit remains "1". If this bit is not reset to "0" even after the elapse of several time cycles, write "0" to this bit to terminate querying.

Writing of such data that both this bit and PING bit go to "1" is protected.

PING (PING) bit (bit 7)

[Function] This bit issues the PING instruction.

When "1" is written to this bit, the PIN instruction is issued to CUnet stations at the station addresses set to the TS0 to TS5 bits. This bit is reset to "0" after completion of issuing.

Writing of data such that both this bit and TQ bit go to "1" is protected.

station TYPe (TYP0 to TYP4) bit (bits 8 to 12)

[Function] These bits set the type codes in Table 5-3 when the function (query), which detects other CUnet station modes, is completed.

Table 5-3 Type Codes at Query Completion

Type codes set to bits 8 to 12	CUnet IC mode	Status of frame option
00H	MEM mode	0
01H	MEM mode	1
02H	IO mode	0
03H	IO mode	1
04H	Unsubstantial MEM mode due to owned expansion	---
05H to 1FH	Reserved	

5.21 New Final Station Register (NFSR)

Address: 352H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	---	---	---	---	---	NFS5	NFS4	NFS3	NFS2	NFS1	NFS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This is a register where a new FS (Final Station) value is written when performing resizing.

Resizing is performed when a hexadecimal NFS value is written to the NFS0 to NFS5 (New Final Station) bits of this register.

When this device (MKY43) is not in the RUN phase, writing to this register is ignored. When the value written to this register is a value to exclude the self-station owned area, writing to the register is ignored (refer to ***"4.4.2.2 Rejection of Resizing"***).

This register changes to "00H" when it finishes sending four resizing instruction to the communication line.

This register also changes to "00H" when the resize overlap occurs or the network stops.

For details of resizing, refer to ***"4.4.2 Resizing of Cycle Time"***.

5.22 Final Station Register (FSR)

Address: 354H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	---	---	---	---	---	---	---	---	---	FS5	FS4	FS3	FS2	FS1	FS0
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[Functional description]

This is a read-only register where hexadecimal FS (Final Station) values are stored in its FS0 to FS5 (Final Station) bits.

5.23 Basic Control Register (BCR)

Address: 356H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LFS	---	OWN5	OWN4	OWN3	OWN2	OWN1	OWN0	BPS1	BPS0	SA5	SA4	SA3	SA2	SA1	SA0
Initial value:	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register stores the basic settings for the MKY43 used to build a CUnet. This register can be written only when the GMM bit (bit 15) of the SCR (System Control Register) is "1".

● **Bit description**

Station Address (SA0 to SA5) bit (bits 0 to 5)

[Function] The Station Addresses (SAs) are set to these bits.

BPS (BPS0, 1) bit (bits 6, 7)

[Function] The baud rates are set to these bits.

Table 5-4 shows the relationship between bit values and baud rates.

Table 5-4 Bit Values and Baud Rates (for 48-MHz Clock)

Bit 7: BPS1	Bit 6: BPS0	Baud rate
1	1	12 Mbps
1	0	6 Mbps
0	1	3 Mbps
0	0	EXC input clock × 1/4

OWN width (OWN0 to OWN5) bit (bits 8 to 13)

[Function] The block count of owned width (OWN width) are set to these bits.

Long Frame Select (LFS) bit (bit 15)

[Function] The frame option of the MKY43 is set to this bit.

When "1" is written to this bit, the frame option is set.

Only "1" can be written to this bit.

To set this bit value to "0", activate a hardware reset.

For details on the frame option, refer to ***"4.4.9 Frame Option [for HUB]"***.

Caution When "0" is written to all bits of OWN0 to OWN5, OWN0 bit is set to "1".

5.24 INTerrupt 0 Control Register (INT0CR)

Address: 358H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	JD	PR	RO	BD	LNG	LOK	MC	RSTR	RSTP	RC	MGNC	MGNE	MSF	MR	DR	ALM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register enables the interrupt trigger generating function of the #INT0 pin. When "1" is written to the bit corresponding to the interrupt source required by the user system of the interrupt sources defined in the bits of the INT0CR, the function of the #INT0 pin is enabled.

● **Bit description**

ALarM (ALM) bit (bit 0)

[Function] This bit enables interrupt trigger occurrence when the station time during cycles reaches the time prespecified to the IT0CR (Interrupt Timing 0 Control Register).

Data Renewal (DR) bit (bit 1)

[Function] This bit enables interrupt trigger occurrence when the data transition of the Memory Block (MB) corresponding to the detection bit preset to the DRCR (Data Renewal Check Register) is detected at the time prespecified to the IT0CR (Interrupt Timing 0 Control Register).
When the same bit value of the INT1CR (INTerrrupt 1 Control Register) is "1", writing "1" to this bit is protected.

Mail Receive (MR) bit (bit 2)

[Function] This bit enables interrupt trigger occurrence when mail reception is completed.

Mail Send Finish (MSF) bit (bit 3)

[Function] This bit enables interrupt trigger occurrence when mail sending is terminated (correctly or incorrectly).

Member Group Not Equal (MGNE) bit (bit 4)

[Function] This bit enables interrupt trigger occurrence by the result of "MGR ≠ MFR".

Member Group Not Collect (MGNC) bit (bit 5)

[Function] This bit enables interrupt trigger occurrence by the result of "MGR > MFR".

Resize Complete (RC) bit (bit 6)

[Function] This bit enables interrupt trigger occurrence when the resizing of a self-station requested from other CUnet stations is completed.

Run SToP (RSTP) bit (bit 7)

[Function] This bit enables interrupt trigger occurrence when the network stops.

Run STaRt (RSTR) bit (bit 8)

[Function] This bit enables interrupt trigger occurrence when the phase changes to the RUN phase.

Member Change (MC) bit (bit 9)

[Function] This bit enables interrupt trigger occurrence when the number of bits at "1" in the MFR (Member Flag Register) increases or decreases.
During interrupt trigger occurrence by this factor, all bits of the RFR (Receive Flag Register), all bits of the LFR (Link Flag Register), and bit 12 (LOK: Link group OK) of the SSR (System Status Register) freeze.

Link group OK (LOK) bit (bit 10)

[Function] This bit enables interrupt trigger occurrence by the result of "Link OK".
During interrupt trigger occurrence by this factor, all bits of the RFR, all bits of the LFR, and bit 12 (LOK) of the SSR freeze.

Link group No Good (LNG) bit (bit 11)

[Function] This bit enables interrupt trigger occurrence by the result of "Link NG (No Good)".
During interrupt trigger occurrence by this factor, all bits of the RFR, all bits of the LFR, and bit 12 (LOK) of the SSR freeze.

Break Detect (BD) bit (bit 12)

[Function] This bit enables interrupt trigger occurrence when break packets sent from other CUnet stations are received.

Resize Overlap (RO) bit (bit 13)

[Function] This bit enables interrupt trigger occurrence when a resize overlap occurs.

Ping Receive (PR) bit (bit 14)

[Function] This bit enables interrupt trigger occurrence when the PING instruction is received from other CUnet stations.

Jammer Detect (JD) bit (bit 15)

[Function] This bit enables interrupt trigger occurrence when a jammer is detected.

5.25 INTerrupt 1 Control Register (INT1CR)

Address: 35AH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	JD	PR	RO	BD	LNG	LOK	MC	RSTR	RSTP	RC	MGNC	MGNE	MSF	MR	DR	ALM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register enables the interrupt trigger generating function of the #INT1 pin. When "1" is written to the bit corresponding to the interrupt source required by the user system of the interrupt sources defined in the bits of the INT1CR, the function of the #INT1 pin is enabled.

● **Bit description**

ALarM (ALM) bit (bit 0)

[Function] This bit enables interrupt trigger occurrence when the station time during cycles reaches the time prespecified to the IT1CR (Interrupt Timing 1 Control Register).

Data Renewal (DR) bit (bit 1)

[Function] This bit enables interrupt trigger occurrence when the data transition of the Memory Block (MB) corresponding to the detection bit preset to the DRCR (Data Renewal Check Register) is detected at the time prespecified to the IT1CR (Interrupt Timing 1 Control Register).
When the same bit value of the INT0CR (INTerrupt 0 Control Register) is "1", writing "1" to this bit is protected.

Mail Receive (MR) bit to Jammer Detect (JD) bit (bits 2 to 15)

[Function] For these bits, refer to the explanation of the same bit in ***"5.24 INTerrupt 0 Control Register (INT0CR)"***.

5.26 Interrupt Timing 0 Control Register (IT0CR)

Address: 35CH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	DR6	DR5	DR4	DR3	DR2	DR1	DR0	---	ALM6	ALM5	ALM4	ALM3	ALM2	ALM1	ALM0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register sets the occurrence timing of DR (Data Renewal) and ALM (ALarM) interrupt triggers in the interrupt trigger generation function of the #INT0 pin. These interrupt triggers occur when the setting value matches the station time.

● **Bit description**

ALarM (ALM0 to ALM6) bit (bits 0 to 6)

[Function] These bits set the occurrence timing of an ALM interrupt trigger.

Values of "0 to 127 (00H to 7FH)" can be written to these bits. However, the station time value in a CUnet must be a value stored in the FSR (Final Station Register) with up to "2" added. When numerical values exceeding these values are written, an interrupt trigger does not occur. Do not write an incorrect value.

Data Renewal (DR0 to DR6) bit (bits 8 to 14)

[Function] These bits set the occurrence timing of a DR interrupt trigger.

Values of "0 to 127 (00H to 7FH)" can be written to them. However, the station time value in a CUnet must be a value stored in the FSR with up to "2" added. When numerical values exceeding these values are written, an interrupt trigger does not occur. Do not write an incorrect value.

5.27 Interrupt Timing 1 Control Register (IT1CR)

Address 35EH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	---	DR6	DR5	DR4	DR3	DR2	DR1	DR0	---	ALM6	ALM5	ALM4	ALM3	ALM2	ALM1	ALM0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register sets the occurrence timing of DR and ALM interrupt triggers in the interrupt trigger generation function of the #INT1 pin. These interrupt triggers occur when the setting value matches the station time.

● **Bit description**

ALarM (ALM0 to ALM6) bit (bits 0 to 6), and Data Renewal (DR0 to DR6) bit (bits 8 to 14)

[Function] For these bits, refer to the explanation of the same bit in ***"5.26 Interrupt Timing 0 Control Register (IT0CR)"***.

5.28 INTerrupt 0 Status Register (INT0SR)

Address: 360H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	JD	PR	RO	BD	LNG	LOK	MC	RSTR	RSTP	RC	MGNC	MGNE	MSF	MR	DR	ALM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register indicates the interrupt factor generated by the interrupt trigger generation function of the #INT0 pin. A bit corresponding to the generated interrupt factor changes to "1". The user system program can determine which interrupt factor triggered an interrupt by reading this register.

When all the bits of this register go to "0", the #INT0 pin returns to keep its High-level output.

To clear a bit indicating "1" of this register to "0", write "1" to the bit (writing "0" is ignored).

● **Bit description**

ALarM (ALM) bit (bit 0)

[Function] This bit indicates that an interrupt trigger occurs when the station time during cycles reaches the time prespecified to the IT0CR (Interrupt Timing 0 Control Register).

Data Renewal (DR) bit (bit 1)

[Function] This bit indicates that an interrupt trigger occurs when the data transition of the Memory Block (MB) corresponding to the detection bit preset to the DRCR (Data Renewal Check Register) is detected at the time prespecified to the IT0CR (Interrupt Timing 0 Control Register).

Mail Receive (MR) bit (bit 2)

[Function] This bit indicates that an interrupt trigger occurs when mail reception is completed.

Mail Send Finish (MSF) bit (bit 3)

[Function] This bit indicates that an interrupt trigger occurs when mail sending is terminated (correctly or incorrectly).

Member Group Not Equal (MGNE) bit (bit 4)

[Function] This bit indicates that an interrupt trigger occurs by the result of "MGR ≠ MFR".

Member Group Not Collect (MGNC) bit (bit 5)

[Function] This bit indicates that an interrupt trigger occurs by the result of "MGR > MFR".

Resize Complete (RC) bit (bit 6)

[Function] This bit indicates an interrupt trigger occurs when the resizing of a self-station requested from other CUnet stations is completed.

Run SToP (RSTP) bit (bit 7)

[Function] This bit indicates that an interrupt trigger occurs when the network stops.

Run STaRt (RSTR) bit (bit 8)

[Function] This bit indicates that an interrupt trigger occurs when the phase changes to the RUN phase.

Member Change (MC) bit (bit 9)

[Function] This bit indicates that an interrupt trigger occurs when the number of bits at "1" in the MFR (Member Flag Register) increases or decreases.

Link group OK (LOK) bit (bit 10)

[Function] This bit indicates that an interrupt trigger occurs by the result of "Link OK".

Link group No Good (LNG) bit (bit 11)

[Function] This bit enables an interrupt trigger that occurs by the result of "Link NG (No Good)".

Break Detect (BD) bit (bit 12)

[Function] This bit indicates that an interrupt trigger occurs when break packets sent from other CUnet stations are received.

Resize Overlap (RO) bit (bit 13)

[Function] This bit indicates that an interrupt trigger occurs when a resize overlap occurs.

Ping Receive (PR) bit (bit 14)

[Function] This bit indicates that an interrupt trigger occurs when the PING instruction is received from other CUnet stations.

Jammer Detect (JD) bit (bit 15)

[Function] This bit indicates that an interrupt trigger occurs when a jammer is detected.

5.29 INTerrupt 1 Status Register (INT1SR)

Address: 362H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	JD	PR	RO	BD	LNG	LOK	MC	RSTR	RSTP	RC	MGNC	MGNE	MSF	MR	DR	ALM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This register indicates the interrupt factor generated by the interrupt trigger generaton function of the #INT1 pin. The bit corresponding to the generated interrupt factor changes to "1". The user system program can determine which interrupt factor triggered an interrupt by reading this register.

When all the bits of this register go to "0", the #INT1 pin returns to keep its High-level output.

To clear a bit indicating "1" of this register to "0", write "1" to the bit (writing "0" is ignored).

● **Bit description**

ALarM (ALM) bit (bit 0)

[Function] This bit indicates that an interrupt trigger occurs when the station time during cycles reaches the time prespecified to the IT1CR (Interrupt Timing 1 Control Register).

Data Renewal (DR) bit (bit 1)

[Function] This bit indicates that an interrupt trigger occurs when the data transition of the Memory Block (MB) corresponding to the detection bit preset to the DRCR (Data Renewal Check Register) is detected at the time prespecified to the IT1CR (Interrupt Timing 1 Control Register).

Mail Receive (MR) bit (bit 2)

[Function] This bit indicates that an interrupt trigger occurs when mail reception is completed.

Mail Send Finish (MSF) bit (bit 3)

[Function] This bit indicates that an interrupt trigger occurs when mail sending is terminated (correctly or incorrectly).

Member Group Not Equal (MGNE) bit (bit 4)

[Function] This bit indicates that an interrupt trigger occurs by the result of "MGR ≠ MFR".

Member Group Not Collect (MGNC) bit (bit 5)

[Function] This bit indicates that an interrupt trigger occurs by the result of "MGR > MFR".

Resize Complete (RC) bit (bit 6)

[Function] This bit indicates an interrupt trigger occurs when the resizing of a self-station requested from other CUnet stations is completed.

Run SToP (RSTP) bit (bit 7)

[Function] This bit indicates that an interrupt trigger occurs when the network stops.

Run STaRt (RSTR) bit (bit 8)

[Function] This bit indicates that an interrupt trigger occurs when the phase changes to the RUN phase.

Member Change (MC) bit (bit 9)

[Function] This bit indicates that an interrupt trigger occurs when the number of bits at "1" in the MFR (Member Flag Register) increases or decreases.

Link group OK (LOK) bit (bit 10)

[Function] This bit indicates that an interrupt trigger occurs by the result of "Link OK".

Link group No Good (LNG) bit (bit 11)

[Function] This bit enables an interrupt trigger that occurs by the result of "Link NG (No Good)".

Break Detect (BD) bit (bit 12)

[Function] This bit indicates that an interrupt trigger occurs when break packets sent from other CUnet stations are received.

Resize Overlap (RO) bit (bit 13)

[Function] This bit indicates that an interrupt trigger occurs when a resize overlap occurs.

Ping Receive (PR) bit (bit 14)

[Function] This bit indicates that an interrupt trigger occurs when the PING instruction is received from other CUnet stations.

Jammer Detect (JD) bit (bit 15)

[Function] This bit indicates that an interrupt trigger occurs when a jammer is detected.

5.30 System Status Register (SSR)

Address: 364H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MC	NM	LNG	LOK	DR	BD	JD	RO	MSE	MR	MGNC	MGNE	---	---	---	---
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R

[Functional description]

This register stores various status in network operation (for details of the starting point of status management, or the time to update some bits of this register, refer to ***"4.2.3.2 Starting Point of Status Management and Exception"***).

● **Bit description**

Member Group Not Equal (MGNE) bit (bit 4)

[Function] This bit indicates "MGR ≠ MFR" when any of the bits of the MGR is "1".
"1" is set to this bit when the bit status of the MFR (Member Flag Register) does not match the bit status of the MGR (Member Group Register) at the "starting point of status management". "0" is set to this bit otherwise.

Member Group Not Collect (MGNC) bit (bit 5)

[Function] This bit indicates "MGR > MFR" when any of the bits of the MGR is "1".
"1" is set to this bit when any of the bits of the MFR corresponding to the MGR at "1" is "0" at the "starting point of status management". It is set to "0" otherwise.

Mail Received (MR) bit (bit 6)

[Function] This bit indicates completion of mail reception.
"1" is set to this bit when the MRB0 (Mail Receive Buffer 0) or MRB1 (Mail Receive Buffer 1) completes the reception of dataset by mail.
When the RCV (ReCeiVed) bits of the MR0CR (Mail Receive 0 Control Register) and MR1CR (Mail Receive 1 Control Register) are cleared to "0", this bit is also cleared to "0".

Mail Send Error (MSE) bit (bit 7)

[Function] This bit indicates that mail sending is terminated with an error.
"1" is set to this bit when an error occurs during mail sending. When all bits of the MESR (Mail Error Status Register) are cleared to "0", this bit is also cleared to "0".

Resize Overlap (RO) bit (bit 8)

[Function] This bit indicates "detection of a resize overlap".
"1" is set to this bit when resizing of a self-station overlaps resizing of other CUnet stations and is disabled. When "1" is written to this bit, it is cleared to "0".

Jammer Detect (JD) bit (bit 9)

[Function] This bit indicates the “jammer detection”.
“1” is set to this bit when a jammer is detected. When “1” is written to this bit, it is cleared to “0”.

Break Detect (BD) bit (bit 10)

[Function] This bit indicates “detection of CUnet station in the BREAK phase”.
When a break packet sent by other CUnet stations was received, “1” is set to this bit. When “1” is written to this bit, it is cleared to “0”.

Data Renewal (DR) bit (bit 11)

[Function] This bit indicates “detection of data transition in global memory”.
“1” is set to this bit when data transition is detected in the memory block corresponding to the DRCR (Data Renewal Check Register) at “1”. The transition timing of this bit from “1” to “0” depends on the MKY43 usage environment. Refer to ***“4.2.4.3 Transition Timing of DR Flag Bit and DRFR Bits from “1” to “0”***.
This flag freezes during the output of the DR (Data Renewal) interrupt trigger. For details on freeze, refer to ***“4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation”***.

Link group OK (LOK) bit (bit 12)

[Function] This bit indicates the “Link OK”.
“1” is set to this bit when all bits of the LFR (Link Flag Register) corresponding to the bit of the LGR (Link Group Register) are “1”.
This bit is cleared to “0” at the “starting point of status management”. However, this bit freezes during output of ALM (ALarM), MC (Member Change), LOK (Link group OK), and LNG (Link group No Good) interrupt triggers. For details of freeze, refer to ***“4.5.7 Register Freezing in Synchronization with Interrupt Trigger Generation”***.

Link group No Good (LNG) bit (bit 13)

[Function] This bit indicates the “Link NG (No Good)”.
“1” is set to this bit when any of the bits of the LFR corresponding to the bit of the LGR at “1” is “0” at the “starting point of status management”. “0” is set to this bit otherwise.

New Member (NM) bit (bit 14)

[Function] This bit indicates member increase.
“1” is set to this bit when any of the bits of the MFR changes from “0” to “1” at the “starting point of status management”. It is set to “0” otherwise.

Member Care (MC) bit (bit 15)

[Function] This bit indicates “member decrease”.
“1” is set to this bit when any of the bits of the MFR changes from “1” to “0” at the “starting point of status management”. “0” is set to this bit otherwise.

5.31 System Control Register (SCR)

Address: 366H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GMM	LF	SNF	OC	BRK	CALL	RUN	START	---	ST6	ST5	ST4	ST3	ST2	ST1	ST0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

[Functional description]

This register controls a CUnet network.

● **Bit description**

Station Time (ST0 to ST6) bit (bits 0 to 6)

[Function] The station time is set to these bits.
The current station time (hexadecimal) is set.
The bit values change dynamically as a cycle passes through.
For details of the station time, refer to ***"4.1.7 Detailed Timing during Cycle"*** and ***"CUnet Introduction Guide"***.

START (START) bit (bit 8)

[Function] This bit controls the network start and stop.
When "1" is written to this bit, the network starts.
This bit keeps "1" during network operation.
A network can be stopped intentionally by writing "0" when this bit is "1".

RUN phase (RUN) bit (bit 9)

[Function] This bit indicates the phase of this device (MKY43).
This bit keeps "1" in the RUN phase.

CALL phase (CALL) bit (bit 10)

[Function] This bit indicates the phase of this device (MKY43).
This bit keeps "1" in the CALL phase.

BReaK phase (BRK) bit (bit 11)

[Function] This bit indicates the phase of this device (MKY43).
This bit keeps "1" in the BREAK phase.

Out of Cycle (OC) bit (bit 12)

[Function] This bit indicates that the network is stopped due to OC (Out Of Cycle).
When the network is stopped due to OC, "1" is set to this bit.
This bit is cleared to "0" when "1" is written to bit 8 (START) or when a hardware reset is activated. For details on OC, refer to ***"4.1.8 Network Stop"***.

Station Not Found (SNF) bit (bit 13)

[Function] This bit indicates that a network is stopped due to SNF (Station Not Found).
When a network is stopped due to SNF, "1" is set to this bit.
This bit is cleared to "0" when "1" is written to bit 8 (START) or when a hardware reset is activated. For details on SNF, refer to ***"4.1.8 Network Stop"***.

Long Frame (LF) bit (bit 14)

[Function] This bit indicates the status of a frame option.
This bit keeps "1" when a frame option is set.
For details on the frame option, refer to ***"4.4.9 Frame Option [for HUB]"***.

Global Memory Monitor (GMM) bit (bit 15)

[Function] This bit operates the GMM function.
"1" can be written to this bit only when bit 8 (START) is "0".
When "1" is written to this bit, this device (MKY43) operates as a GMM station.
This bit must be "1" when writing data to the BCR (Basic Control Register). For details of GMM, refer to ***"4.4.8 Global Memory Monitor (GMM) Function"***.

5.32 Chip Code Register (CCR)

Address: 368H

Bit:	15-8	7-0
	4BH "K"	4DH "M"
R/W:	R	R

Address: 36AH

Bit:	15-8	7-0
	34H "4"	59H "Y"
R/W:	R	R

Address: 36CH

Bit:	15-8	7-0
	5FH "_"	33H "3"
R/W:	R	R

Address: 36EH

Bit:	15-8	7-0
	30H "0"	76H "v"
R/W:	R	R

[Functional description]

This register can read a byte-type ASCII code "MKY43_v0" from a little endian CPU. It is a read-only register to check whether the MKY43 is embedded. If the ASCII code is read from a big endian CPU, a different character string is read.

5.33 Read Hazard Protection Buffer 0 (RHPB0)

Address: 370H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RHPB0 15	RHPB0 14	RHPB0 13	RHPB0 12	RHPB0 11	RHPB0 10	RHPB0 9	RHPB0 8	RHPB0 7	RHPB0 6	RHPB0 5	RHPB0 4	RHPB0 3	RHPB0 2	RHPB0 1	RHPB0 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 372H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RHPB0 31	RHPB0 30	RHPB0 29	RHPB0 28	RHPB0 27	RHPB0 26	RHPB0 25	RHPB0 24	RHPB0 23	RHPB0 22	RHPB0 21	RHPB0 20	RHPB0 19	RHPB0 18	RHPB0 17	RHPB0 16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 374H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RHPB0 47	RHPB0 46	RHPB0 45	RHPB0 44	RHPB0 43	RHPB0 42	RHPB0 41	RHPB0 40	RHPB0 39	RHPB0 38	RHPB0 37	RHPB0 36	RHPB0 35	RHPB0 34	RHPB0 33	RHPB0 32
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 376H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RHPB0 63	RHPB0 62	RHPB0 61	RHPB0 60	RHPB0 59	RHPB0 58	RHPB0 57	RHPB0 56	RHPB0 55	RHPB0 54	RHPB0 53	RHPB0 52	RHPB0 51	RHPB0 50	RHPB0 49	RHPB0 48
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[Functional description]

The 64-bit Memory Block (MB) data in the Global Memory (GM) is collectively copied to this buffer when the read hazard protection function is controlled.

When the MB addresses ("00H to 3FH") of the copy source are written to RHCR0 (Read Hazard Control Register 0), the data in the memory block of the copy source is copied to this buffer.

5.34 Read Hazard Protection Buffer 1 (RHPB1)

Address: 378H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RHPB1 15	RHPB1 14	RHPB1 13	RHPB1 12	RHPB1 11	RHPB1 10	RHPB1 9	RHPB1 8	RHPB1 7	RHPB1 6	RHPB1 5	RHPB1 4	RHPB1 3	RHPB1 2	RHPB1 1	RHPB1 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 37AH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RHPB1 31	RHPB1 30	RHPB1 29	RHPB1 28	RHPB1 27	RHPB1 26	RHPB1 25	RHPB1 24	RHPB1 23	RHPB1 22	RHPB1 21	RHPB1 20	RHPB1 19	RHPB1 18	RHPB1 17	RHPB1 16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 37CH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RHPB1 47	RHPB1 46	RHPB1 45	RHPB1 44	RHPB1 43	RHPB1 42	RHPB1 41	RHPB1 40	RHPB1 39	RHPB1 38	RHPB1 37	RHPB1 36	RHPB1 35	RHPB1 34	RHPB1 33	RHPB1 32
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Address: 37EH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RHPB1 63	RHPB1 62	RHPB1 61	RHPB1 60	RHPB1 59	RHPB1 58	RHPB1 57	RHPB1 56	RHPB1 55	RHPB1 54	RHPB1 53	RHPB1 52	RHPB1 51	RHPB1 50	RHPB1 49	RHPB1 48
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

[Functional description]

The 64-bit Memory Block (MB) data in the Global Memory (GM) is collectively copied to this buffer when the read hazard protection function is controlled.

When the MB addresses ("00H to 3FH") of the copy source are written to RHCR1 (Read Hazard Control Register 1), the data in the memory block of the copy source is copied to this buffer.

5.35 Write Hazard Protection Buffer 0 (WHPB0)

Address: 380H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WHPB0 15	WHPB0 14	WHPB0 13	WHPB0 12	WHPB0 11	WHPB0 10	WHPB0 9	WHPB0 8	WHPB0 7	WHPB0 6	WHPB0 5	WHPB0 4	WHPB0 3	WHPB0 2	WHPB0 1	WHPB0 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 382H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WHPB0 31	WHPB0 30	WHPB0 29	WHPB0 28	WHPB0 27	WHPB0 26	WHPB0 25	WHPB0 24	WHPB0 23	WHPB0 22	WHPB0 21	WHPB0 20	WHPB0 19	WHPB0 18	WHPB0 17	WHPB0 16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 384H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WHPB0 47	WHPB0 46	WHPB0 45	WHPB0 44	WHPB0 43	WHPB0 42	WHPB0 41	WHPB0 40	WHPB0 39	WHPB0 38	WHPB0 37	WHPB0 36	WHPB0 35	WHPB0 34	WHPB0 33	WHPB0 32
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 386H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WHPB0 63	WHPB0 62	WHPB0 61	WHPB0 60	WHPB0 59	WHPB0 58	WHPB0 57	WHPB0 56	WHPB0 55	WHPB0 54	WHPB0 53	WHPB0 52	WHPB0 51	WHPB0 50	WHPB0 49	WHPB0 48
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This buffer stores the data for one memory block (64 bits, that is, 8 bytes) in the write hazard protection function.

The 64-bit data of this buffer is collectively written when the MB addresses ("00H to 3FH") of the write destination are written to WHCR0 (Write Hazard Control Register 0).

Caution When the START bit of the SCR (System Control Register) is "1", if the specified MB is other than the self owned area, the MB is write protected and the data is not written to the GM. For the GM write protection, refer to (1) in ***"4.1.5 Protection against Misoperation"***.

5.36 Write Hazard Protection Buffer 1 (WHPB1)

Address: 388H

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WHPB1 15	WHPB1 14	WHPB1 13	WHPB1 12	WHPB1 11	WHPB1 10	WHPB1 9	WHPB1 8	WHPB1 7	WHPB1 6	WHPB1 5	WHPB1 4	WHPB1 3	WHPB1 2	WHPB1 1	WHPB1 0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 38AH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WHPB1 31	WHPB1 30	WHPB1 29	WHPB1 28	WHPB1 27	WHPB1 26	WHPB1 25	WHPB1 24	WHPB1 23	WHPB1 22	WHPB1 21	WHPB1 20	WHPB1 19	WHPB1 18	WHPB1 17	WHPB1 16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 38CH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WHPB1 47	WHPB1 46	WHPB1 45	WHPB1 44	WHPB1 43	WHPB1 42	WHPB1 41	WHPB1 40	WHPB1 39	WHPB1 38	WHPB1 37	WHPB1 36	WHPB1 35	WHPB1 34	WHPB1 33	WHPB1 32
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Address: 38EH

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WHPB1 63	WHPB1 62	WHPB1 61	WHPB1 60	WHPB1 59	WHPB1 58	WHPB1 57	WHPB1 56	WHPB1 55	WHPB1 54	WHPB1 53	WHPB1 52	WHPB1 51	WHPB1 50	WHPB1 49	WHPB1 48
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

[Functional description]

This buffer stores the data for one memory block (64 bits, that is, 8 bytes) in the write hazard protection function is controlled.

The 64-bit data of this buffer is collectively written when the MB addresses ("00H to 3FH") of the write destination are written to WHCR1 (Write Hazard Control Register 1).

Caution When the START bit of the SCR (System Control Register) is "1", if the specified MB is other than the self owned area, the MB is write protected and the data is not written to the GM. For the GM write protection, refer to (1) in ***"4.1.5 Protection against Misoperation"***.

Chapter 6 Ratings

This chapter describes the ratings of the MKY43.

6.1 Electrical Ratings 6-3
6.2 AC Characteristics 6-3
6.3 Package Dimensions 6-7
6.4 Recommended Soldering Conditions 6-8
6.5 Recommended Reflow Conditions 6-8

Chapter 6 Ratings

This chapter describes the ratings of the MKY43.

6.1 Electrical Ratings

Table 6-1 lists the absolute maximum ratings of the MKY43.

Table 6-1 Absolute Maximum Ratings (Vss = 0 V)

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	-0.3 to +4.6	V
Input voltage	Vi	Vss-0.3 to +6.0	V
Output voltage	Vo	Vss-0.3 to +6.0	V
Signal pin input current	Ii	-6 to +6	mA
Peak output current (Type-D pin)	Iop	±8	mA
Peak output current (Type-C, -E, -F pins)	Iop	±16	mA
Allowable power dissipation	PT	345	mW
Operating temperature	Topr	-40 to +85	°C
Storage temperature	Tstg	-65 to +150	°C

Table 6-2 lists the electrical ratings of the MKY43.

Table 6-2 Electrical Ratings (T_A = 25 °C Vss = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating power supply voltage	V_{DD}	---	3.0	3.3	3.6	V
Mean operating current	$V_{DD}A$	Vi = V_{DD} or Vss f = 50 MHz output open	---	29	75	mA
External input frequency	Fclk	Input to Xi pin	---	48	50	MHz
Input pin capacitance	Ci	V_{DD} = Vi = 0 V f = 1 MHz T_A = 25°C	---	6	---	pF
Output pin capacitance	Co		---	9	---	pF
I/O pin capacitance	Ci/o		---	10	---	pF
Rise/fall time of input signal	T_{IRF}	---	---	---	20	ns
Rise/fall time of input signal	T_{IRF}	Schmitt trigger input	---	---	30	µs

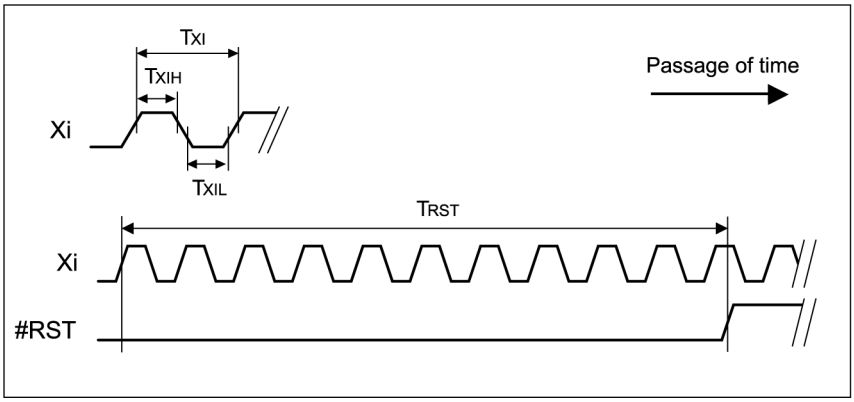
6.2 AC Characteristics

Table 6-3 lists the measurement conditions for AC characteristics of the MKY43.

Table 6-3 AC Characteristics Measurement Conditions

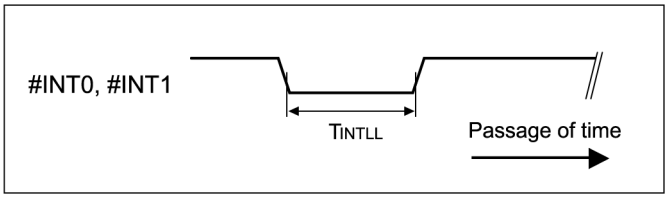
Symbol	Name	Typ.	Unit
C_{OL}	Output load capacitance	80	pF
V_{DD}	Power supply voltage	3.3	V
T_A	Temperature	25	°C

6.2.1 Clock and Reset Timing



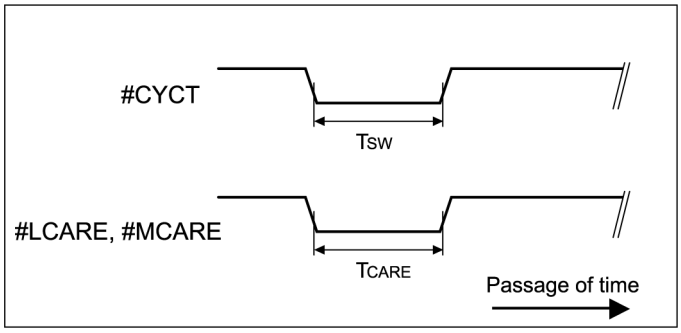
Symbol	Name	Min.	Max.	Unit
TXI	Clock period width	20	---	ns
TXIH	Clock High level width	5	---	ns
TXIL	Clock Low level width	5	---	ns
TRST	Reset enable Low level width	10 × TXI	---	ns

6.2.2 Output Timing of Interrupt Trigger



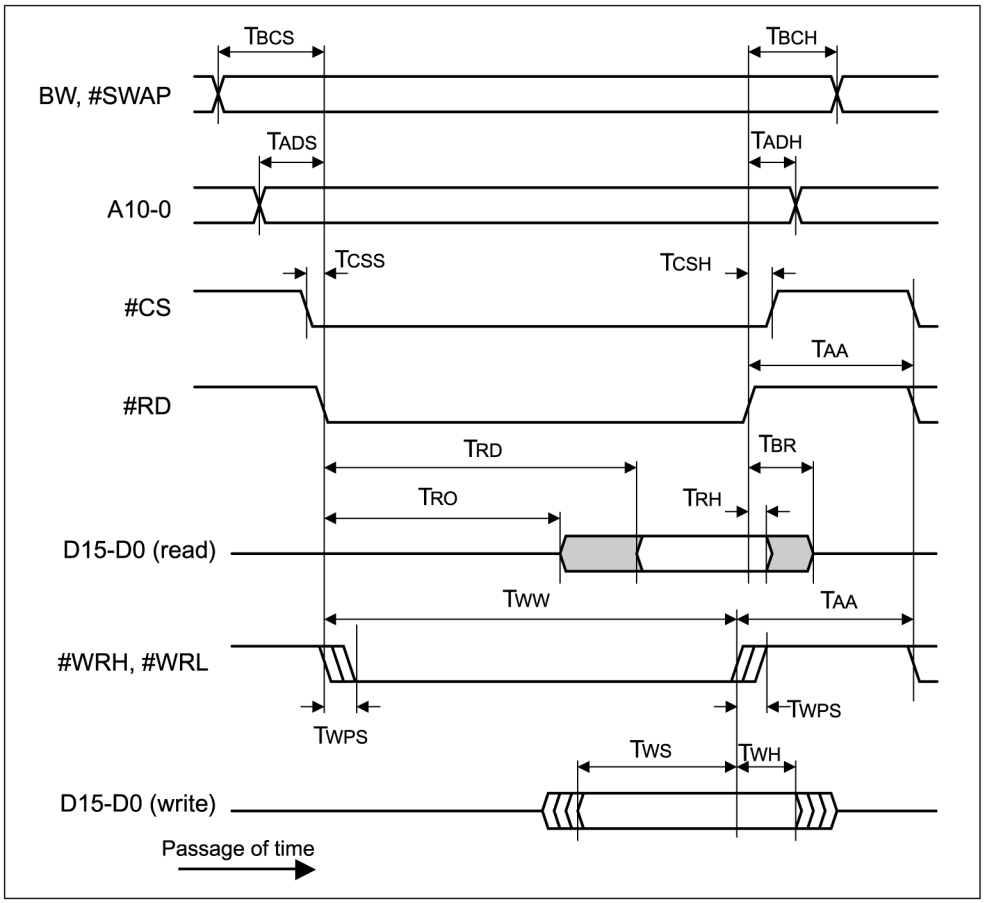
Symbol	Name	Min.	Max.	Unit
TINTLL	Pin Low level width	10 × TXI	---	ns

6.2.3 Output Timing of #CYCT, #LCARE and #MCARE



Symbol	Signal	Min.	Typ.	Max.	Unit
TSW	#CYCT pin output Low level width	1.8 × TBPS	2 × TBPS	2.2 × TBPS	ns
TCARE	CARE pulse Low level width (Retriggerable one-shot multi-vibrator output)	2505728 × TXI (Approx. 52.2 ms: 48 Mhz)	---	---	ns

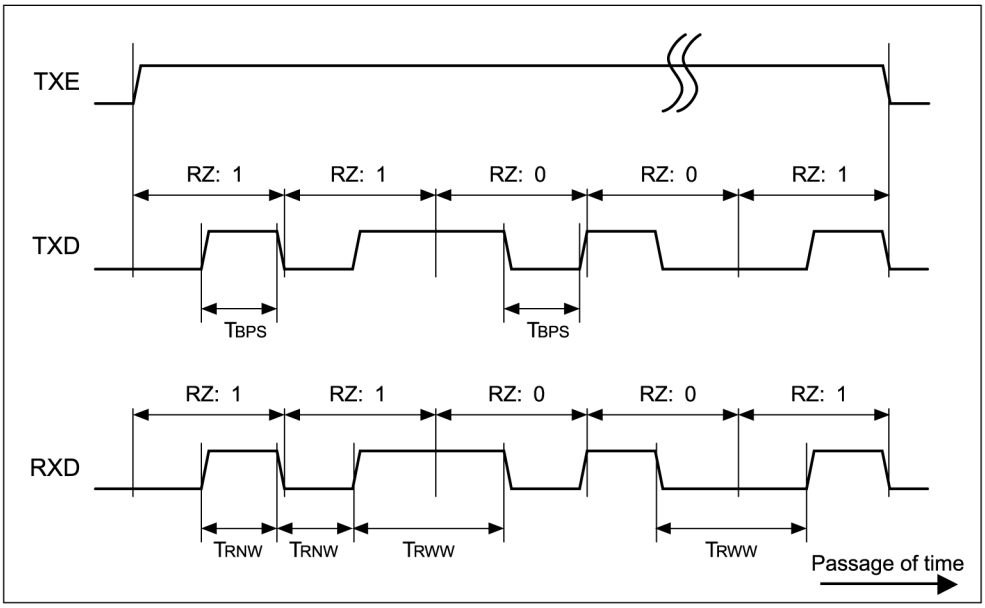
6.2.4 Read/Write Timing



Symbol	Name	Min.	Typ.	Max.	Unit
TBCS	Bus change setup	0	---	---	ns
TBCH	Bus change hold	0	---	---	ns
TADS	Address setup	0	---	---	ns
TADH	Address hold	0	---	---	ns
TCSS	CS Setup	0	---	---	ns
TCSH	CS Hold	0	---	---	ns
TAA	Access to access	42 (2 × Txi)	---	---	ns
TRO	Read to out (bus drive)	47 ((2 × Txi) + 5)	---	---	ns
TRD	Read to data (valid data output)	---	---	89 ((4 × Txi) + 5)	ns
TRH	Read data hold	2.5	---	---	ns
TBR	Bus release	5	7.5	10	ns
TWW	Write signal width	63 (3 × Txi)	---	---	ns
TWPS	Allowable error between write signals (#WRH and #WRL)	---	---	20 (1 × Txi)	ns
TWS	Write data setup	10	---	---	ns
TWH	Write data hold	0	---	---	ns

(Driving clock 48 MHz: Txi = 20.83 ns)

6.2.5 Baud Rate Timing

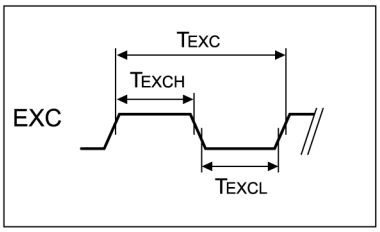


Symbol	Baud rate	Short pulse width of sending signal	Unit
TBPS	12 Mbps	≈83.33 ±5	ns
	6 Mbps	≈166.67 ±5	ns
	3 Mbps	≈333.33 ±5	ns

(Driving clock 48 MHz: Txi = 20.83 ns)

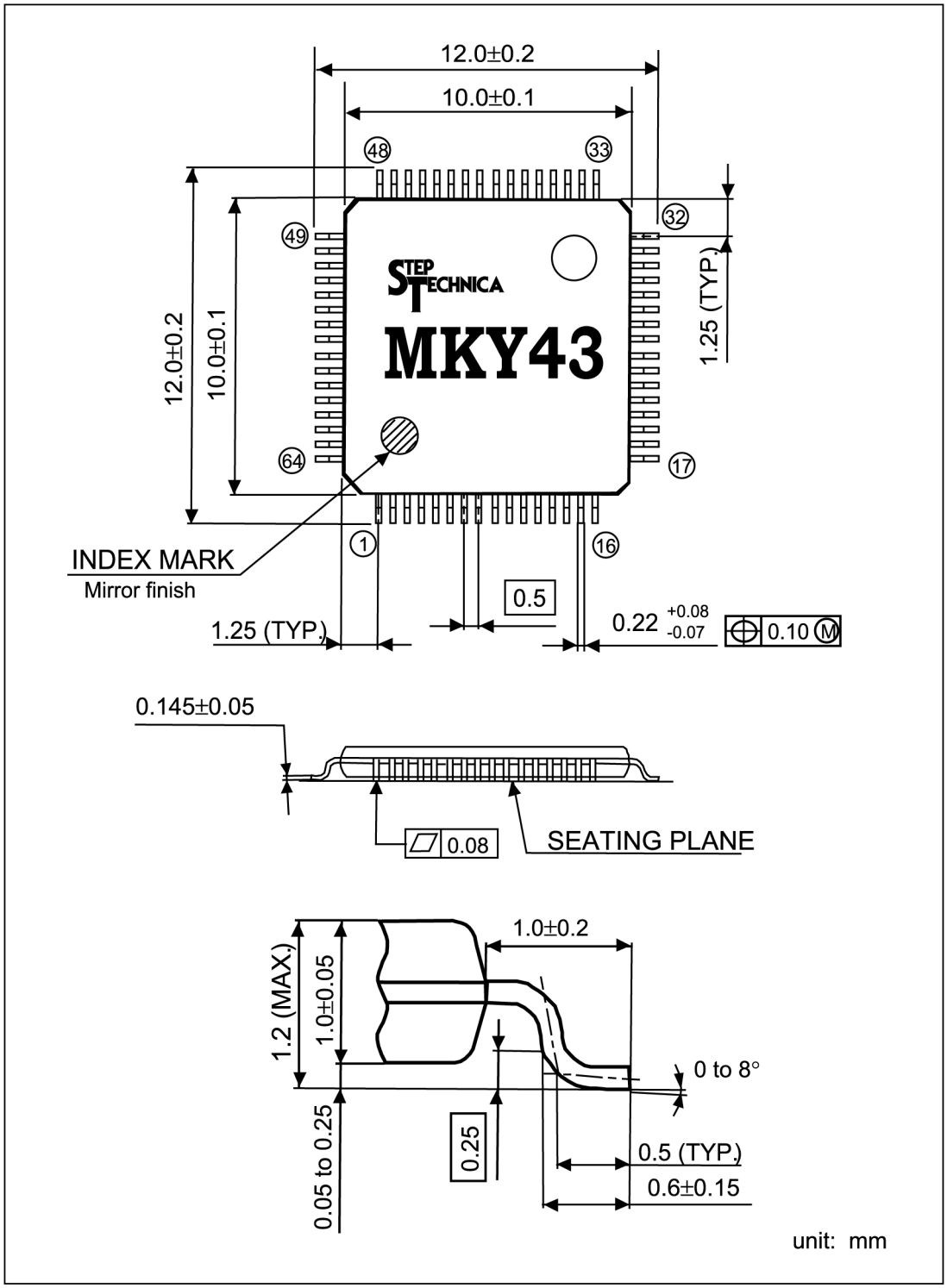
Symbol	Name	Min.	Typ.	Max.	Remarks
TRNW	Short pulse width of input signal	0.51 × TBPS	1.0 × TBPS	1.49 × TBPS	Allowable pulse width as RZ signal
TRWW	Long pulse width of input signal	1.51 × TBPS	2.0 × TBPS	2.49 × TBPS	Allowable pulse width as RZ signal

6.2.6 External Baud Rate Clock (EXC) Timing



Symbol	Name	Min.	Max.	Unit
TEXC	External baud rate clock period width	4 × TXI	---	ns
TEXCH	External baud rate clock High level width	1.5 × TXI	---	ns
TEXCL	External baud rate clock Low level width	1.5 × TXI	---	ns

6.3 Package Dimensions



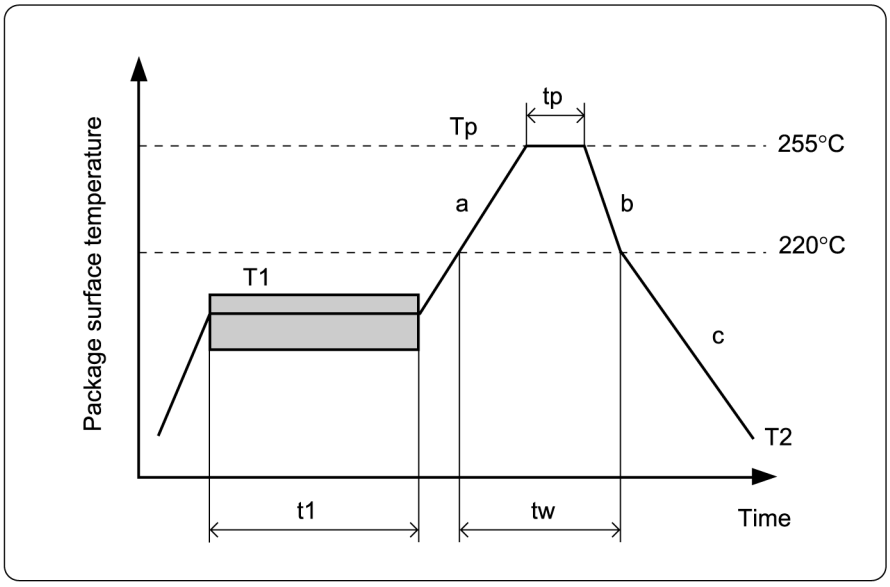
6.4 Recommended Soldering Conditions

Parameter	Symbol	Reflow	Manual soldering iron
Peak temperature (resin surface)	Tp	255°C max.	380°C max.
Peak temperature holding time	tp	10 s max.	5 s max.

Caution

(1) Product storage conditions: TA = 40°C max., RH = 85% for prevention of moisture absorption
(2) Manual soldering: Temperature of the tip of soldering iron 380°C, 5 s max.
(Device lead temperature 260°C, 10 s max., package surface temperature 150°C)
(3) Reflow: Twice max.
(4) Flux: Non-chlorine flux (should be cleaned sufficiently)
(5) Ultrasonic cleaning: Depending on frequencies and circuit board shapes, ultrasonic cleaning may cause resonance, affecting lead strength

6.5 Recommended Reflow Conditions



Parameter	Symbol	Value
Pre-heat (time)	t1	60 to 80/s
Pre-heat (temperature)	T1	150 to 190°C
Temperature rise rate	a	1°C to 4°C/s
Peak condition (time)	tp	10 s max.
Peak condition (temperature)	Tp	255°C
Cooling rate	b	to 1.5°C/s
Cooling rate	c	to 0.5°C/s
High temperature area	tw	220°C, 60 s max.
Removal temperature	T2	≦ 100°C

Caution

The recommended conditions apply to hot-air reflow or infrared reflow. Temperature indicates resin surface temperature of the package.

Appendix

Appendix 1 Cycle Time Table App-3

Appendix 2 Differences between MKY43 and MKY40 .....App-4

Appendix 3 Processing when Network Stop by OC (Out of Cycle) Occurs App-7

Appendix 1 Cycle Time Table

(unit: μs)

	Typ. (LF = 0)			Frame option (LF = 1)		
FS	12 Mbps	6 Mbps	3 Mbps	12 Mbps	6 Mbps	3 Mbps
1 (01H)	102.00	204.00	408.00	172.00	344.00	688.00
2 (02H)	128.33	256.67	513.33	215.83	431.67	863.33
3 (03H)	155.00	310.00	620.00	260.00	520.00	1,040.00
4 (04H)	182.00	364.00	728.00	304.50	609.00	1,218.00
5 (05H)	209.33	418.67	837.33	349.33	698.67	1,397.33
6 (06H)	237.00	474.00	948.00	394.50	789.00	1,578.00
7 (07H)	265.00	530.00	1,060.00	440.00	880.00	1,760.00
8 (08H)	293.33	586.67	1,173.33	485.83	971.67	1,943.33
9 (09H)	322.00	644.00	1,288.00	532.00	1,064.00	2,128.00
10 (0AH)	351.00	702.00	1,404.00	578.50	1,157.00	2,314.00
11 (0BH)	380.33	760.67	1,521.33	625.33	1,250.67	2,501.33
12 (0CH)	410.00	820.00	1,640.00	672.50	1,345.00	2,690.00
13 (0DH)	440.00	880.00	1,760.00	720.00	1,440.00	2,880.00
14 (0EH)	470.33	940.67	1,881.33	767.83	1,535.67	3,071.33
15 (0FH)	501.00	1,002.00	2,004.00	816.00	1,632.00	3,264.00
16 (10H)	532.00	1,064.00	2,128.00	864.50	1,729.00	3,458.00
17 (11H)	563.33	1,126.67	2,253.33	913.33	1,826.67	3,653.33
18 (12H)	595.00	1,190.00	2,380.00	962.50	1,925.00	3,850.00
19 (13H)	627.00	1,254.00	2,508.00	1,012.00	2,024.00	4,048.00
20 (14H)	659.33	1,318.67	2,637.33	1,061.83	2,123.67	4,247.33
21 (15H)	692.00	1,384.00	2,768.00	1,112.00	2,224.00	4,448.00
22 (16H)	725.00	1,450.00	2,900.00	1,162.50	2,325.00	4,650.00
23 (17H)	758.33	1,516.67	3,033.33	1,213.33	2,426.67	4,853.33
24 (18H)	792.00	1,584.00	3,168.00	1,264.50	2,529.00	5,058.00
25 (19H)	826.00	1,652.00	3,304.00	1,316.00	2,632.00	5,264.00
26 (1AH)	860.33	1,720.67	3,441.33	1,367.83	2,735.67	5,471.33
27 (1BH)	895.00	1,790.00	3,580.00	1,420.00	2,840.00	5,680.00
28 (1CH)	930.00	1,860.00	3,720.00	1,472.50	2,945.00	5,890.00
29 (1DH)	965.33	1,930.67	3,861.33	1,525.33	3,050.67	6,101.33
30 (1EH)	1,001.00	2,002.00	4,004.00	1,578.50	3,157.00	6,314.00
31 (1FH)	1,037.00	2,074.00	4,148.00	1,632.00	3,264.00	6,528.00
32 (20H)	1,073.33	2,146.67	4,293.33	1,685.83	3,371.67	6,743.33
33 (21H)	1,110.00	2,220.00	4,440.00	1,740.00	3,480.00	6,960.00
34 (22H)	1,147.00	2,294.00	4,588.00	1,794.50	3,589.00	7,178.00
35 (23H)	1,184.33	2,368.67	4,737.33	1,849.33	3,698.67	7,397.33
36 (24H)	1,222.00	2,444.00	4,888.00	1,904.50	3,809.00	7,618.00
37 (25H)	1,260.00	2,520.00	5,040.00	1,960.00	3,920.00	7,840.00
38 (26H)	1,298.33	2,596.67	5,193.33	2,015.83	4,031.67	8,063.33
39 (27H)	1,337.00	2,674.00	5,348.00	2,072.00	4,144.00	8,288.00
40 (28H)	1,376.00	2,752.00	5,504.00	2,128.50	4,257.00	8,514.00
41 (29H)	1,415.33	2,830.67	5,661.33	2,185.33	4,370.67	8,741.33
42 (2AH)	1,455.00	2,910.00	5,820.00	2,242.50	4,485.00	8,970.00
43 (2BH)	1,495.00	2,990.00	5,980.00	2,300.00	4,600.00	9,200.00
44 (2CH)	1,535.33	3,070.67	6,141.33	2,357.83	4,715.67	9,431.33
45 (2DH)	1,576.00	3,152.00	6,304.00	2,416.00	4,832.00	9,664.00
46 (2EH)	1,617.00	3,234.00	6,468.00	2,474.50	4,949.00	9,898.00
47 (2FH)	1,658.33	3,316.67	6,633.33	2,533.33	5,066.67	10,133.33
48 (30H)	1,700.00	3,400.00	6,800.00	2,592.50	5,185.00	10,370.00
49 (31H)	1,742.00	3,484.00	6,968.00	2,652.00	5,304.00	10,608.00
50 (32H)	1,784.33	3,568.67	7,137.33	2,711.83	5,423.67	10,847.33
51 (33H)	1,827.00	3,654.00	7,308.00	2,772.00	5,544.00	11,088.00
52 (34H)	1,870.00	3,740.00	7,480.00	2,832.50	5,665.00	11,330.00
53 (35H)	1,913.33	3,826.67	7,653.33	2,893.33	5,786.67	11,573.33
54 (36H)	1,957.00	3,914.00	7,828.00	2,954.50	5,909.00	11,818.00
55 (37H)	2,001.00	4,002.00	8,004.00	3,016.00	6,032.00	12,064.00
56 (38H)	2,045.33	4,090.67	8,181.33	3,077.83	6,155.67	12,311.33
57 (39H)	2,090.00	4,180.00	8,360.00	3,140.00	6,280.00	12,560.00
58 (3AH)	2,135.00	4,270.00	8,540.00	3,202.50	6,405.00	12,810.00
59 (3BH)	2,180.33	4,360.67	8,721.33	3,265.33	6,530.67	13,061.33
60 (3CH)	2,226.00	4,452.00	8,904.00	3,328.50	6,657.00	13,314.00
61 (3DH)	2,272.00	4,544.00	9,088.00	3,392.00	6,784.00	13,568.00
62 (3EH)	2,318.33	4,636.67	9,273.33	3,455.83	6,911.67	13,823.33
63 (3FH)	2,365.00	4,730.00	9,460.00	3,520.00	7,040.00	14,080.00

Appendix 2 Differences between MKY43 and MKY40

The MKY43 was developed as a product inheriting the MEM mode function of the MKY40 (5 V) which is a CUnet Family Station-IC product. The function and operation of the MKY43 as a CUnet Family-IC are the same as the MKY40, but in actually using the MKY43, note the following points:

- 3.3-V single power supply (5-V tolerant signal pin). The power consumption can be reduced by 60% or more than the MKY40.
- Small package: 64 pins, 0.5-mm pitch, 10 × 10 mm: TQFP
- The 16-/8-bit, 3.3-V/5-V TTL level CPU bus can be connected.
- The memory maps and each register address are different from those of the MKY40.

Register Function Compatibility List

(◎: Full compatible. ○: Partially different.)

Address value	Area name	Register name	Bit count	Target function	Compatibility with MKY40
300H to 307H	RFR	Receive Flag Register	64	Link detection	○
308H to 30FH	LFR	Link Flag Register	64		○
310H to 317H	MFR	Member Flag Register	64	Member detection	○
318H to 31FH	DRFR	Data Renewal Flag Register	64	Data transition detection	◎
320H to 327H	LGR	Link Group Register	64	Link detection	◎
328H to 32FH	MGR	Member Group Register	64	Member detection	◎
330H to 337H	DRCR	Data Renewal Check Register	64	Data transition detection	◎
338H	RHCR0	Read Hazard Control Register 0	16	Read hazard protection	New
33AH	RHCR1	Read Hazard Control Register 1	16		New
33CH	WHCR0	Write Hazard Control Register 0	16	Write hazard protection	New
33EH	WHCR1	Write Hazard Control Register 1	16		New
340H	MSLR	Mail Send Limit time Register	16	Mail sending	◎
342H	MSSR	Mail Send Result Register	16		◎
344H	MESR	Mail Error Status Register	16		◎
346H	MSCR	Mail Send Control Register	16		◎
348H	MR0CR	Mail Receive 0 Control Register	16	Mail reception	○
34AH	MR1CR	Mail Receive 1 Control Register	16		○
34CH	CCTR	Care CounTer Register	16	System support	◎
34EH	UTCR	UTility pin Control Register	16		New
350H	QCR	Query Control Register	16		◎
352H	NFSR	New Final Station Register	16	System	○
354H	FSR	Final Station Register	16		◎
356H	BCR	Basic Control Register	16		◎
358H	INT0CR	INTerrupt 0 Control Register	16	Interrupt control	◎
35AH	INT1CR	INTerrupt 1 Control Register	16		◎
35CH	IT0CR	Interrupt Timing 0 Control Register	16		◎
35EH	IT1CR	Interrupt Timing 1 Control Register	16		◎
360H	INT0SR	INTerrupt 0 Status Register	16		◎
362H	INT1SR	INTerrupt 1 Status Register	16		◎
364H	SSR	System Status Register	16	System	○
366H	SCR	System Control Register	16		○
368H to 36FH	CCR	Chip Code Register	64		◎
370H to 377H	RHPB0	Read Hazard Protection Buffer 0	64	Read hazard protection	New
378H to 37FH	RHPB1	Read Hazard Protection Buffer 1	64		New
380H to 387H	WHPB0	Write Hazard Protection Buffer 0	64	Write hazard protection	New
388H to 38FH	WHPB1	Write Hazard Protection Buffer 1	64		New

Differences in Hardware

Item	MKY43	MKY40
Power supply voltage	3.3 V	5.0 V
Package	0.5-mm pitch 64 pins TQFP	0.5-mm pitch 100 pins TQFP
Bus pin level	3.3-V TTL (5-V tolerant) (3.3-V TTL level CPU bus can be connected.) (5.0-V TTL level CPU bus can be connected.)	5-V TTL level (It is possible to connect only the 5.0 V system TTL level CPU bus.)
Bus width	16 bit / 8 bit	32 bit / 16 bit / 8 bit
Byte write when 16-bit user bus is connected	Byte write is not supported. (Set both #WRH pin and #WRL pin Low.)	Byte write is supported.
Interrupt pin	#INT0, #INT1	#INT0, #INT1, #INT2
Port Out bit of SSR Care Pulse bit of BCR	Not provided	PO0, PO1, PO2, PO3, (SSR) CP (BCR)
Setting pin for address, etc. (Initial value of BCR is written)	Not provided	#SA0 to #SA5, #OWN0 to #OWN5, BPS0, BPS1
IO mode function	Not provided	Provided (The MODE pin is provided.)
CYCT output, PING output (CYCT is equivalent to STB)	#CYCT signal and #PING signal can be output to UTY1 pin and UTY2 pin.	#STB signal and PING signal are output to #STB pin and PING pin respectively
UTCR (UTility pin Control Register)	Added for controlling UTY1 pin and UTY2 pin. (Set this register by selecting from among Hi-Z, #CYCT output, and #PING output.)	----------
Driving clock	Clock input to the Xi pin (The oscillator is not supported.)	Clock input to the Xi pin. Or the crystal oscillator between the Xi pin and Xo pin can be supported.
TXD pin output during reset period	Low level	Clock frequency obtained by dividing the driving clock by 32
Hazard protection	Hazard-protection-buffer method	Window-lock method
Memory map	Different from that of the MKY40	----------
Address of each register	Different from that of the MKY40	----------
Bus access time	T_{RD} (max) 89 ns	T_{RD} (max) 130 ns
Operating current (max)	75 mA	130 mA

● Hazard protection function

Protection method against data hazards at read/write access, which occur due to the user CPU bus width, was changed. In the MKY43, the two GM windows, which the MKY40 has, were integrated into one GM and the window lock was abolished. Therefore, in the MKY43, the window lock and the related registers in the MKY40 were removed and the hazard protection function is newly used. The hazard protection function can be utilized as follows.

★ At the time of read: When the Memory Block (MB: "00H to 3FH") addresses of the copy source are written to RHCR0 (Read Hazard Control Register 0), the 64-bit data of the MB is collectively copied to RHPB0 (Read Hazard Protection Buffer 0). Users can refer to data-hazard-free 64-bit data by reading the RHPB0. The RHCR1 and RHPB1 also operate in the same way as the RHCR0 and RHPB0.

★ At the time of write: Regarding the 64-bit data to be written to one MB, write all the data for 64 bits to WHPB0 (Write Hazard Protection Buffer 0). The 64-bit data in the WHPB0 is collectively written to the MB of the copy destination by writing the MB address of the copy destination to WHCR0 (Write Hazard Control Register 0). The WHCR1 and WHPB1 also operate in the same way as the WHCR0 and WHPB0.

Differences in Functions (Overview)

Item	MKY43	MKY40
Break Detect of SSR	Full-time detection	Detected only in RUN phase
Resize Overlap of SSR	Detection is performed except when NFSR is "00H"	Detection is performed regardless of NFSR value
MGNE and MGNC of SSR	When all of the MGR bits are "0", the result is always "0"	If all of the MGR bits are "0", the result "1" appears
Status at OC stop	If the relation between the Final Station (FS) value and the Station Address (SA) value of the self-station is "(FS - SA) > 2", the statuses of the RFR, LFR, MFR, and #MON pin immediately before the OC stop are hold. If the relation is other than "(FS - SA) > 2", the statuses are the same as shown in the MKY40 column.	RFR: Bits in any place other than the owned area of a self-station change according to the status of receiving packets LFR: Bits in any place other than the owned area of a self-station are "0" MFR: All of the bits are"0" #MON pin: Outputs High level
SNF of SCR	Network is stopped in RUN phase and in BREAK phase	Network is stopped in RUN phase
NFSR	Changes to "00H" when this register finishes sending four resizing instruction to the communication line. Also changes to "00H" when RO occurs or Network stops	Does not change to "00H" upon completion of sending
RFR, LFR	Bits to be self-owned change to "1" when START bit of SCR is set to "1"	Bits to be self-owned except GMM are always "1"
RFR updating operation in GMM mode	Each bit is updated in real time	All of the bits are collectively updated at the lead point of a cycle
Network stop interrupt	Occurs due to START bit of SCR set to "0", SNF stop, or OC stop	Occurs due to SNF stop or OC stop
MSLR	LMFLT (LiMit time FauLT) occurs when the setting is "0003H" or smaller	LMFLT (LiMit time FauLT) occurs when the setting is "0000H"
Write protection for MRB0	When RDY bit or RCV bit of MR0CR is "1"	When START bit of SCR is "1"
Write protection for MRB1	When RDY bit or RCV bit of MR1CR is "1"	
MR0CR, MR1CR	If data is written to the RCV bit or RDY bit, values of bits 0 to 5 (SiZe) and bits 8 to 13 (SRC) are cleared to "00H"	Even if data is written to the RCV bit or RDY bit, values of bits 0 to 5 (SiZe) and bits 8 to 13 (SRC) are retained
Handling of endian	Handling of endian for MKY43 is different from that for MKY40 (see Note 1)	

Note 1: If the MKY43 is adopted for the system which had used the MKY40, or if the program for the system with MKY40 is ported for the system with MKY43, addresses corresponding to given memory area may differ between the MKY40 and the MKY43. Therefore, when using the system mixedly connecting the MKY43 and MKY40 to the network, or when porting the program for the system with MKY40 for the system with MKY43, pay attention to the addresses corresponding to given memory area.

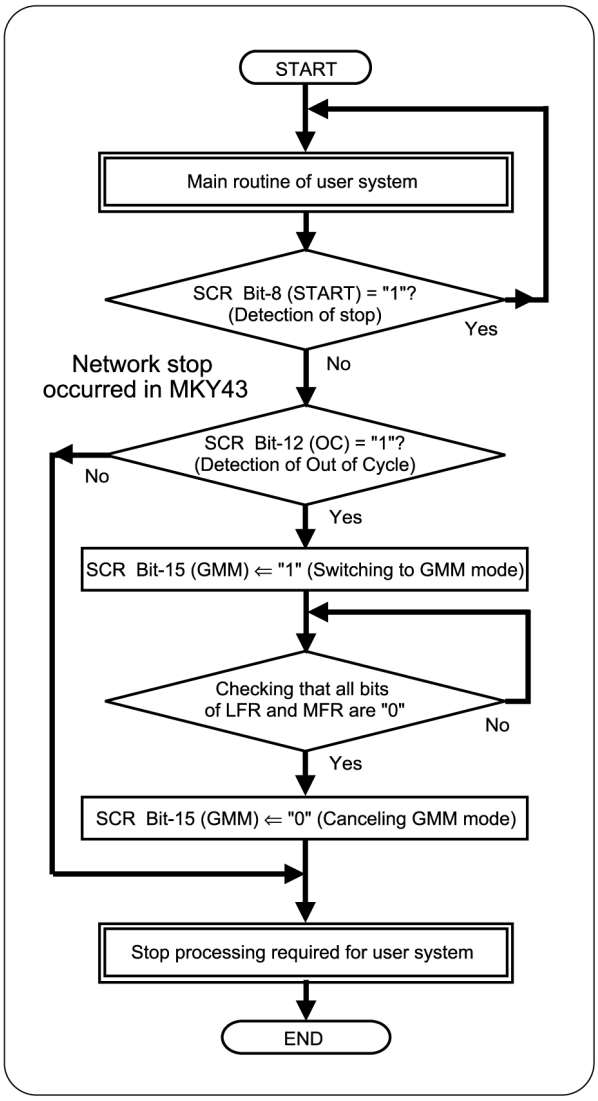
Appendix 3 Processing when Network Stop by OC (Out of Cycle) Occurs

As for the CUnet station, there are two types of network stop as follows: "intended network stop", for which the user writes "0" to the START bit of the SCR in order to stop the network, and "unintended network stop", which occurs due to SNF (Station Not Found) stop and OC (Out of Cycle) stop (for details, refer to ***"4.1.8.1 Details of SNF (Station Not Found)"*** and ***"4.1.8.2 Details of OC (Out of Cycle)"*** respectively). Therefore, network stops must be detected and handled when operating the CUnet station.

In the MKY43, if the OC stop occurs in the state in which the relation between the Final Station (FS) value and the Station Address (SA) value of the self-station is "(FS − SA) > 2", the receiving status (RF: Receive Flag), link status (LF: Link Flag), and member status (MF: Member Flag) immediately before the network stop are held to the Receive Flag Register (RFR), Link Flag Register (LFR), and Member Flag Register (MFR) respectively. Because of this status holding, a Low level is output to the #MON pin when "1" is stored in any of the bits corresponding to CUnet stations other than the self-station of the MFR. If an LED indicator is connected to the #MON pin so that it can go ON when a Low level is output, the LED indicator will go ON. The statuses of RFR, LFR, and MFR immediately before the network stop by OC can be canceled by using any one of the following three methods.

(1) Switching to the GMM function (The status holding is canceled in about one cycle)
(2) Hardware reset
(3) An expanded resizing, through operating network, covering the owned area of the MKY43 which stopped

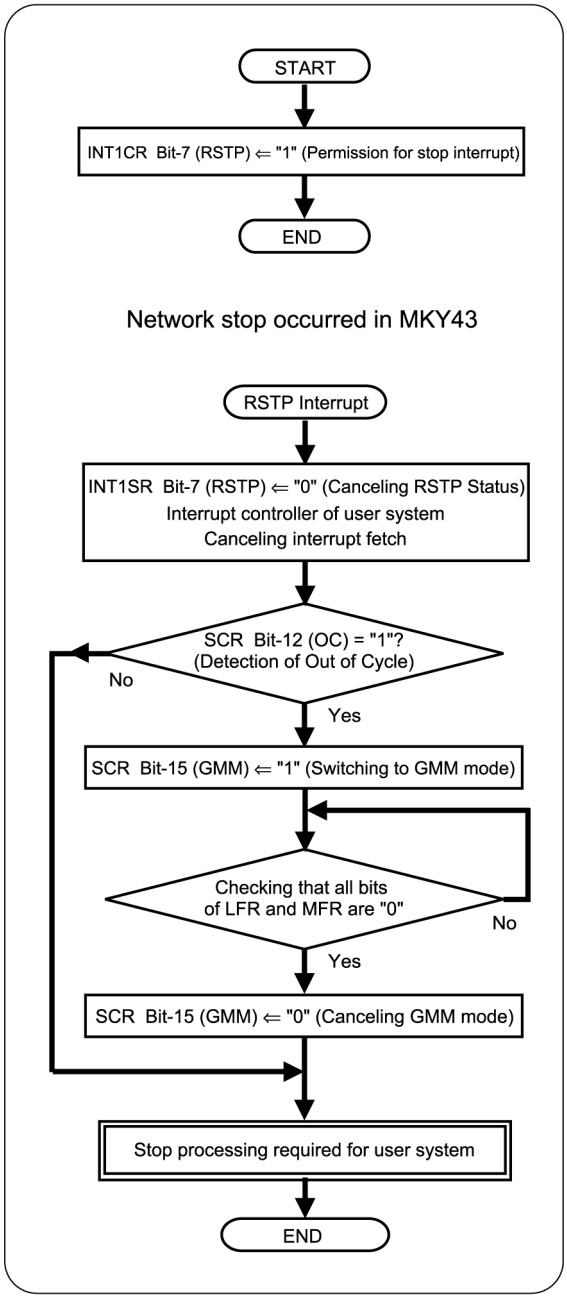
If the status holding is canceled, "0" is stored into all of the bits of LFR and MFR, and a High level is output to the #MON pin. If an LED indicator is connected to the #MON pin so that it can go ON when a Low level is output, the LED indicator will go OFF.



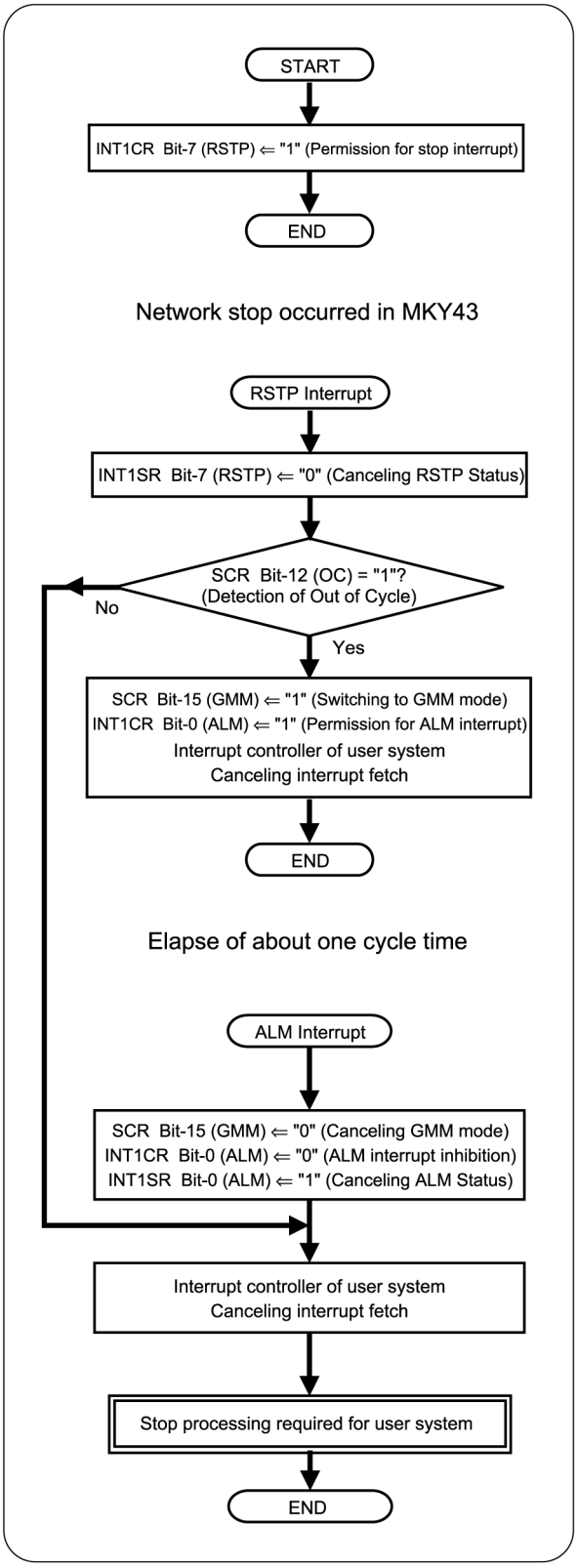
App. Fig. 1 Example of Processing by Polling when Network Stops

Appendix Figures 1 to 3 show examples of algorithms which are intended to detect and control a network stop by using "(1) Switching to the GMM function (The status holding is canceled in about one cycle.)" method above. For details on "START" at the top of figures, refer to ***"4.1.3 Initialization and Start-up of Communication"***.

In addition, if methods (2) and (3) above are used, data of the Global Memory (GM) is not updated upon receiving. However, data of the GM is also updated upon receiving while the GMM function by the method (1) above is operating.


START
INT1CR Bit-7 (RSTP) ⇐ "1" (Permission for stop interrupt)
END
Network stop occurred in MKY43
RSTP Interrupt
INT1SR Bit-7 (RSTP) ⇐ "0" (Canceling RSTP Status)
Interrupt controller of user system
Canceling interrupt fetch
SCR Bit-12 (OC) = "1"?
(Detection of Out of Cycle)
No
Yes
SCR Bit-15 (GMM) ⇐ "1" (Switching to GMM mode)
Checking that all bits
of LFR and MFR are "0"
No
Yes
SCR Bit-15 (GMM) ⇐ "0" (Canceling GMM mode)
Stop processing required for user system
END

App. Fig. 2 Example of Processing
by Using Interrupt when Network Stops (1)


START
INT1CR Bit-7 (RSTP) ⇐ "1" (Permission for stop interrupt)
END
Network stop occurred in MKY43
RSTP Interrupt
INT1SR Bit-7 (RSTP) ⇐ "0" (Canceling RSTP Status)
SCR Bit-12 (OC) = "1"?
(Detection of Out of Cycle)
No
Yes
SCR Bit-15 (GMM) ⇐ "1" (Switching to GMM mode)
INT1CR Bit-0 (ALM) ⇐ "1" (Permission for ALM interrupt)
Interrupt controller of user system
Canceling interrupt fetch
END
Elapse of about one cycle time
ALM Interrupt
SCR Bit-15 (GMM) ⇐ "0" (Canceling GMM mode)
INT1CR Bit-0 (ALM) ⇐ "0" (ALM interrupt inhibition)
INT1SR Bit-0 (ALM) ⇐ "1" (Canceling ALM Status)
Interrupt controller of user system
Canceling interrupt fetch
Stop processing required for user system
END

App. Fig. 3 Example of Processing
by Using Interrupt when Network Stops (2)

Revision History

Version No	Date	Page	Contents
1.1	January, 2009	2-4	Added a referential section to function description of items “#MCARE”, “#LCARE”, and “#MON” in ***Table 2-1***.
		2-6	Made corrections to “i/o” item of “No. 51” and “No. 54” in ***Table 2-2***.
		4-9	Added a “Caution” part about ***Appendix 3***.
		4-21	Modified description of (2) in ***4.2.3.6 Member Group Register (MGR)*** and added a “Caution” part.
		4-31	Added description of “(2)” to the “Caution” part in ***4.3.2 Operation for Mail Reception***.
		4-47	Added a “Caution” part about ***Appendix 3***.
		4-50	Added description to the “Reference” part.
		4-57	Made the sentences of items “MGNE” and “MGNC” in ***Table 4-3*** appropriate.
		5-17, 18	Added the following two sentences to “[Function]” part in “receive ReaDY (RDY) bit (bit 6)” item. “This bit can be operated when the START bit of the SCR is “1”.” “If the START bit of the SCR changes to “0” when this bit is “1”, this bit also changes to “0”.”
		5-32	Added the following description to “[Function]” parts in items “Member Group Not Equal (MGNE) bit (bit 4)” and “Member Group Not Collect (MGNC) bit (bit 5)”. “when any of the bits of the MGR is “1””
		App-6	In the table “Differences in Functions (Overview)”; • Added “MGNE and MGNC of SSR” item. • Added “Status at OC stop” item. • Changed the title of the item “RFR, LFR, MFR” to “RFR, LFR”. • Added “RFR updating operation in GMM mode” item.
		App-7, 8	Added the section, ***Appendix 3 Processing when Network Stop by OC (Out of Cycle) Occurs***.

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